A 2.45GHz POWER HARVESTING CIRCUIT IN 90nm CMOS

G. Giannakas[1], F. Plessas[1,2], G. Nassopoulos[1], and G. Stamoulis[1]

[1]Department of Computer & Communication Engineering, University of Thessaly
Volos, Greece
[2]Department of Electrical and Computer Engineering, University of Patras
Patra, Greece
ggiannac@inf.uth.gr

ABSTRACT

In this work, an overview of the state-of-the-art of the design techniques of power harvesting (rectifying) circuits is presented. The evolution of each circuit, the advantages and design constraints, are investigated and compared. Furthermore, a novel 2.45GHz power-harvesting circuit is implemented in 90nm CMOS. Using voltage and power conversion efficiency as a FOM, the optimum rectifier topology is determined. When input power is -19.73dBm, the proposed rectifier allows improving the Power and the Voltage Conversion Efficiency, achieving a PCE of 14.68% (for R_L=1MΩ) and a VCE of 29.21%.

Index Terms— *RFID; power harvesting; RF-to-DC*

1. INTRODUCTION

Rectifiers or RF-to-DC converters are used in radio frequency identification (RFID) transponders where the energy storage element is powered up by the transmitted RF signal. Diodes or diode-connected MOS transistors are commonly used to implement rectifiers. Full-wave bridge structures are also used as they offer higher power efficiency, smaller output ripples and greater reverse breakdown voltage compared with their counterpart, the half-wave rectifiers. However, they are both constrained by the inherent diode/transistor forward-bias voltage drop which results in a significant power loss within the rectifier, that affects the overall power efficiency and decreases the delivered voltage to the following modules. This negative impact becomes increasingly significant in the design of low-voltage power supplies, which is the case for new sub-micron CMOS technologies. The oldest and predominant topology has been introduced by *J. Dickson* (Voltage Doubler, VD, for DC-DC conversion) and is the most frequently and efficiently used in literature. Another common architecture is the Gate Cross Coupled Rectifier (GCCR). Finally, fully Cross-Coupled structures (NVC) have also been introduced where both upper and lower main branch transistors are cross-coupled.

In this work we develop a novel rectifier circuit using a 90nm CMOS process for 2.45GHz RFID applications where only a few publications exist [1-3]. To compare the performance of the proposed architecture with previously presented schemes we implement each one of these in the process we use. Furthermore, by comparing simulation results from a real-world study with previously reported data, the feasibility of this approach is evaluated. Finally, the proposed scheme includes a resonant voltage boosting network, which provides an adequate amplitude swing from a small signal, a rectifier and a limiter. Starting from the basic calculation results, according to the regulations in Europe (Table I), we will present our conclusions for the microwave band (2450MHz, 500mW) of RFID operation.

TABLE I. VOLTAGE AMPLITUDE FOR A TYPICAL 50 OHM ANTENNA

	RFID link specifications					
	Frequency Band (MHz)	*f_c (MHz)*	*P_{TX} (dBm)*	*FSPL (dB)*	*P_{RX} (dBm)*	*V_{ampl} (mV)*
1	865.0-865.6[4]	865.30	20	51.19[a]	-31.19	8.72
2	865.6-867.5[4]	866.55	33	51.21[a]	-18.21	38.88
3	867.6-868.0[4]	867.80	27	51.22[a]	-24.22	19.46
4	2446-2454[4]	2450.00	27	60.23[a]	-33.23	6.89

a. Working distance of 10m

2. BOOSTING NETWORK

The highest output voltage is achieved at the resonant frequency:

$$f = \frac{1}{2\pi\sqrt{LC}} \ , \qquad (1)$$

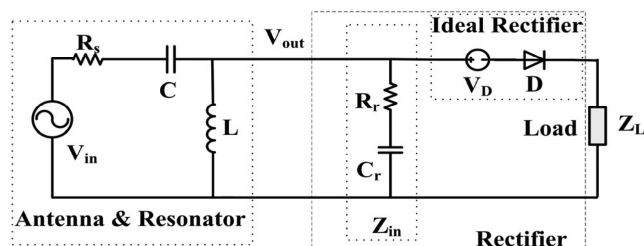

Figure 1. Resonant-Match tank and Rectifier

and is determined by:

$$V_{out} = \frac{1}{R_s} \cdot \sqrt{\frac{L}{C}} . V_{in} \qquad (2)$$

According to (2), the rule of thumb is to make the inductance as large as possible, and choose a suitable capacitance for a given frequency. An important parameter is the quality factor of the inductor, which degrades the performance. This circuit (Fig. 1) plays a dual role to realize resonance at 2.45GHz and to inductively compensate (*L*-match) the input impedance of rectifier (i.e. $Z_{in} \approx 1\text{-}j.13$). The loaded quality factor Q_L of this network, when it is connected to the (20-stages) rectifier under working conditions, was found to be approximately equal to 3.28, as we focused more on matching than tuning to the resonant frequency of 2.45GHz, to achieve large loaded Q_L and avoid impedance mismatch [5].

If V_{out} is the input voltage of the rectifier (at the output of the boosting network) which turns on the MOS (diode connected or switch) transistors and makes effective the rectification of the RF power, then, by taking into account the free-space path losses (FSPL) for the specific application ($G_t = G_r =$ 0dBi, $Q_{Loaded} = 3.28$, $R_s = 50\Omega$, $\lambda = 0.123$m, $P_t =$ 0.5W) we derive:

$$V_{out}(mV) = \frac{69.212 Q_L}{d(m)} = \frac{227.015}{d(m)} \qquad (3)$$

In Fig. 2 the variance of V_{out} is plotted versus the distance from the transmitter.

3. CURRENT SITUATION DESCRIPTION

As is depicted in Fig. 3(a), a voltage doubler consists of a dc-level shifter (M1, C1) and a peak detector (M2, C2) with a voltage boost equal to $2 \cdot N \cdot (V_o\text{-}V_{drop})$ for *N* stages. V_{drop} is the voltage drop caused by threshold and channel resistance of the MOSFET. The DC-DC converter is transformed to an RF-DC converter of *N* stages, by connecting the V_{LOW} of the 1st stage to ground as shown in Fig. 4(b). The same connections are applied in all cascaded types used.

In another architecture, often called as Gate Cross Coupled Rectifier (GCCR), two diode connected MOS and two switching MOS are used. This is a modified version of the bridge full wave rectifier, but lower voltage is required to turn the MOS fully on. A 4-nMOS approach is depicted in Fig. 3(b).

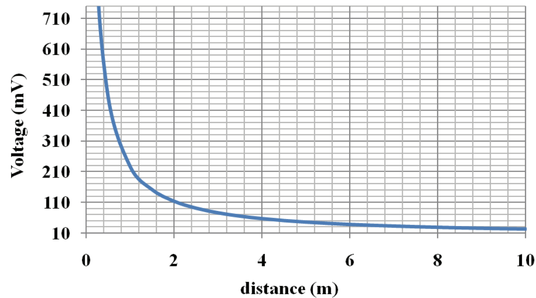

Figure 2. V_{out} versus distance

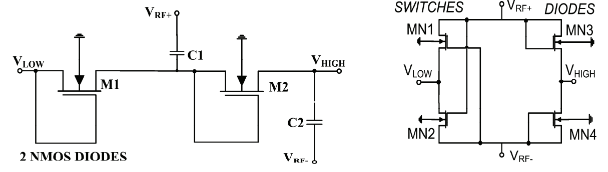

Figure 3. (a) Dickson (VD) basic cell, (b) (GCCR) basic cell

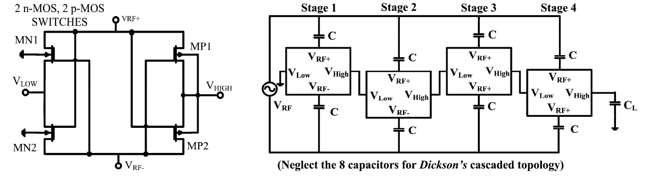

Figure 4. (a) NVC basic cell, (b) General Cascaded topology (N=4)

A third topology, is the fully cross coupled structure named as negative voltage converter (NVC) or H-bridge or 4-transistor cell [6], in which cross coupled n- and p-MOS transistors are used as shown in Fig.4(a). Usually Low-V_{th} MOSFETs are employed for fast switching. A drawback of this topology is the reverse flow of current when $V_{outdc} > V_{in}$, but in contrast to other schemes using diode MOS, no threshold voltage drop exists, because the transistors act as switches. Anyway, a negligible drop occurs due to the small on resistance r_{ds} of MOSFETs. In Fig.4(a), the bulk connections, are used to avoid parasitic bipolar latch-up and leakage currents. Also a cascaded system, depicted in Fig. 4(b), can be formed by series connection of several similar basic cells, for the last two topologies (GCCR, NVC) and almost similarly for the Dickson's, where capacitors to the RF+ and RF- paths must be added to avoid reverse current flow and to control the build-up of large V_{outdc}.

4. V_{TH} REDUCTION & PROPOSED RECTIFIER

Nowadays, although length size (*L*) continuously decreases, V_{th} doesn't scale down with the same rate. Threshold V_{th} is the gate to source voltage which accumulates enough charge into the gate to sustain the depletion region. Due to the lack of power supply in passive tags, the reduction of the "dead zone" of the rectifier has to be performed using techniques that don't need additional power at the start up-state.

Typically the option of multiple threshold voltages is realized by adjusting the thickness of the gate oxide (t_{ox}) or the doping profile in the channel, which complicates fabrication process and requires higher cost. Alternatively, V_{th} can be controlled by the bias voltage at the body (back-gate) terminal. A forward bias on the bulk–source junction (V_{BS}>0) will cause a V_{th} reduction, due to the reverse body effect as shown in Fig. 5(a) [2].

Another technique uses Floating Gate transistors (FG) which imitate the operation of depletion mode transistors. Usually, a (second) control gate is used, which is responsible for the charge transferring control. This is achieved by hot carrier injection through gate oxide or FN (Fowler-Nordheim) tunneling through this control gate [5].

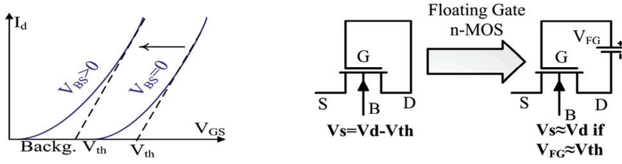

Figure 5. (a) Back-gate (2nd gate) MOS, (b) Floating Gate (FG) NMOS

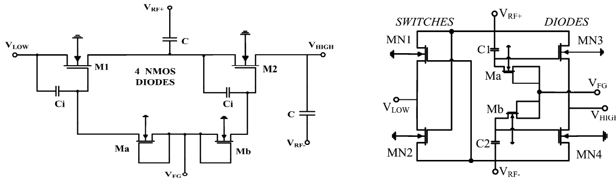

Figure 6. (a) Proposed Dickson VD-FG, (b) Proposed GCCR-FG

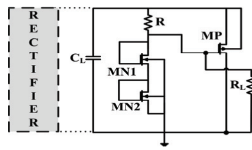

Figure 7. Voltage Limiter (W/L=1um/100nm)

The V_{th} of these FG-MOSFETs can be set after or during fabrication to a specific value, according to the amount of charge that has been injected to the gate.

Based on a basic Voltage Doubler (VD) and on a GCCR, we introduce a modified basic cell the *pseudo-FG* with the addition of two MOS diode connected transistors and two capacitors at the drain-gate connection path as is depicted in Fig. 6(a) and Fig. 6(b). The signal V_{FG} that is essential for the reduction of threshold can be produced by one efficient stage of a NVC or a GCCR basic cell using zero V_{th} (ZVT) MOSFETs. A voltage is inserted in the drain-gate path of the diode connected M1, M2 and if $V_{FG}=V_{th}$, then $V_s=V_d$ as shown in Fig. 5(b). Thus the threshold voltage of the transistors M1, M2 is reduced accordingly to the value of V_{FG}. This approach improves VCE and reduces time delay and ripple. Of course, using this option in near-field ($d < \lambda/2\pi$), a voltage limiter must me employed at the output of the circuit which produces the FG signal, to avoid the appearance of a large voltage in drain-gate connection and hence the increase of V_{th}. In the voltage limiter, the two NMOS diode connected transistors (Fig.7) act as a “zener” diode.

As soon as V_{RF} exceeds the sum of the voltage thresholds of the two NMOS transistors, current starts flowing through R. When $V_R>V_{th,PMOS}$ then the PMOS turns on and additional current flows through the PMOS, to reduce the increase in the output voltage and protect the following modules. This limiter is also used at the output of the 20-stages rectifier that will be presented in the next section (Fig. 8).

5. SIMULATION RESULTS

A series of simulations have been performed to investigate the performance of previously reported rectifiers compared with the proposed one in a 90nm RF-CMOS process. Initially, three different 1-stage rectifier topologies, the GCCR, the NVC and the VD have been simulated, for various threshold voltages V_{th} (e.g. RFMOS: n/420mV, p/-350mV, LVT: n/320mV, p/-260mV, nZVT: -10mV, back-gated). Table II shows the simulation results, where the proposed topology is compared to other classical ones. The proposed VD-FG achieves the best voltage conversion efficiency (VCE = 96% and 93.8%) especially when the FG signal is generated by a NVC-nZVT topology (FG-1) rather than a GCCR-ZVT (FG-8). It should be noted that all topologies have been designed and simulated using the same process and conditions. Between all the VD topologies (Fig. 9 and Table II), the use of a back-gate LVT results in a fine VCE equal to 84.6%, the use of a simple RFMOS results in a VCE equal to 50.6% and the use of a LVT results in a VCE equal to 78.4%. The second proposed topology, the GCCR-FG, achieves a slightly better VCE than the back-gate GCCR, while the GCCR-ZVT achieves the best one. If a 1MΩ load exists, the proposed VD-(FG-8) achieves the best performance between the VDs when is driven (FG signal) by the GCCR-ZVT. This is also true for the 4-stage rectifier.

Finally, a real case rectification circuit is presented able to generate a dc voltage of 1.25V by an extremely low RF input (Fig.10). A VD-ZVT 20-stages rectifier had slightly better performance than other schemes but after some time (μs), the V_{dc} drops out, due to large leakage currents. The NVC-nZVT rectifier (20-stages again) had a similar problem. The main reason is possibly because of the use 2 NMOS switches (of zero V_{th}) and the fact that when the one is closed (opened) the other is not 100% opened (closed). Only the GCCR-ZVT cell doesn’t suffer from this drawback, so this topology has been used in the proposed 20-stages rectifier. Our efforts were focused on achieving a large VCE (Table IV) for W/L=1um/100nm rather than a large PCE. Large MOSFETs are used to sustain large currents (small R_L) needed in a large PCE as in [2, 5]. To generate an output voltage of 1.2V, an input voltage of 180mV is needed when R_L=200kΩ and PCE=23.91%, or 135mV when R_L = 500kΩ and PCE=17% as predicted by (4).

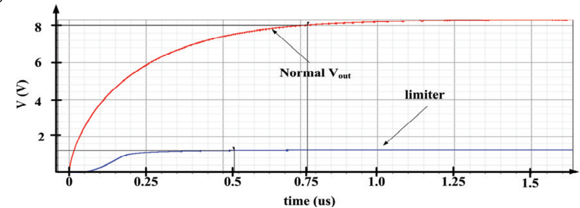

Figure 8. Performance of voltage limiter at the output of a 20-stage rectifier

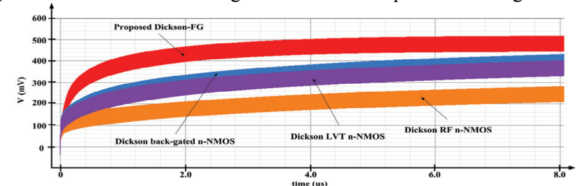

Figure 9. Dickson based, VD, rectifier’s comparison (1 stage)

TABLE II COMPARISON OF RECTIFIERS

1-stage Rectifiers ($V_{in\ rec}$=250mV)				4-stages ($V_{in\ rec}$=250mV)		
Topology (CMOS)	V_{dc} (mV)	$V_{dc\ 1M\Omega}$ (mV)	Delay (us)	V_{dc} (mV)	$V_{dc\ 1M\Omega}$ (mV)	Delay (us)
1. NVC nZVt, pLVt	302	264	.380	1504	560	6
2. NVC Back-g. LVt	277	244	.076	--	--	--
3. NVC LVt	291	256	.082	1598	515	6
4. NVC RF Fet	301	263	.094	--	--	--
5. GCCR LVt	375	186	>10	850	350	8
6. Proposed GCCR LVt	409	266	2.2	932	412	8
7. GCCR Back-g. LVt	406	207	9	--	--	--
8. GCCR n-ZVt	420	405	0.4	1363	1100	.76
9. VD n-LVt	392	124	>9	820	240	>9
10. VD Back-g. LVt	423	137	>9	974	280	>9
11. VD RF Fet	253	58	>10	--	--	--
12. Proposed VD (FG-1)	480	302	5.1	918	400	~5
13. Proposed VD (FG-8)	469	388	5.0	1021	476	~5

TABLE III PERFORMANCE COMPARISON

	F/ $P_{t,eirp}$	V_o/ R_L	PCE/ VCE	S[1] / V_{in}	dist./ Q_L
This work	2.45G 0.5W	1.25V 1M	14.68% 29.21%	-19.73dBm 32.62m	2.12m 3.28
[1] 0.5um	2.45G 4W	1.5V 1M	5.00% ---	-13.47 dBm 67m	2.6m ---
[2] 90nm	2.45G ---	1V 167k	6.67% 20.8%	-0.46 dBm 300m	--- ---
[3] 0.5um	2.45G 4 W	1.2V 1M	37%[2] ---	-25.68 dBm 73.5m	6-12m 3.22
[7] 180nm	0.9G 0.32W	1.8V .47M	4.43% 17.66%	-8.08 dBm 125m	1.1m ---
[5] 250nm	0.92G 4W	2V 1.32M	32%[3] 20%	-22.6 dBm 50m	7-15m 3.9
[6] 180nm	0.95G 4W	0.5V .25M	23.5% ---	-22.4 dBm 33.86m	21.6m ---
[8] 180nm	0.92G 4W	1V .5M	5.14% 28.63%	-14.1 dBm 62.37m	--- ~7

[1]input power, [2]R_s=300Ohm, [3] at -8dBm input power

TABLE IV PERFORMANCE SUMMARY (20- STAGES GCCR-ZVT)

Without Resistive Load			With Resistive Load R_L=1MΩ			
$V_{in\ rec}$[1] (mV)	V_{out} (V)	VCE %	V_{out} (V)	PCE[2] %	VCE %	S (dBm)
66	1.25	45.5	0.57	8.00	21.60	-23.93
100	2.35	58.8	1.07	12.32	26.80	-20.03
250	6.75	67.5	3.78	24.59	37.80	-12.35
300	8.20	68.3	5.82	40.49	40.17	-10.77
500	15.0	75.0	9.80	41.33	49.00	-6.34

[1]$V_{in\ rec}$ is the voltage at the input of the rectifier (after the boosting network)
[2]Due to Q_L, $V_{in\ rec}$ is divided by 3.28 to calculate the total PCE.

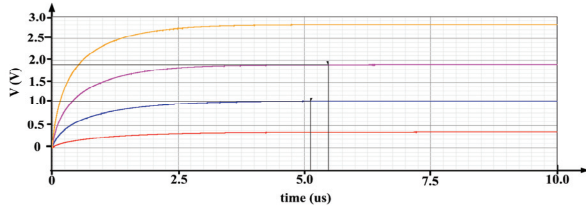

Figure 10. DC output Voltage of the proposed GCCR (N=20, R_L=1MΩ) when $V_{in\ rec}$ varies from 50 to 200mV

200fF MIM capacitors have been used within the rectifier and also for the capacitive load C_L. In a real implementation, C_L must be larger, e.g. 200pF to store enough energy for the tag. In this case, a tag active for 20μs, can develop a power almost equal to 8μW, but with a larger time delay. It should be noted that Power and Voltage Conversion Efficiency (PCE, VCE) are determined by:

$$PCE = \frac{P_{dcout}}{P_{RFin}} = \frac{2R_s V_{dc}^2}{R_L V_o^2} \quad \& \quad VCE = \frac{V_{dc}}{2NQ_L V_o} \qquad (4)$$

where $2N$ is the gain of a cascaded VD of N stages and Q_L the loaded quality factor (resonator and rectifier). Tables III and IV give a performance comparison and a performance summary of the proposed rectification scheme respectively. It is obvious that the proposed architecture is more efficient and robust compared to previously reported works, especially when taking into account, the transmitted (eirp) power, the frequency of operation (FSPL), the antenna gains and radiation resistance R_s, and the load R_L.

6. CONCLUSIONS

For passive autonomous (self-powered) RFID tags, low cost is a crucial factor. With the aid of the proposed technique of threshold reduction, better performance is achieved using CMOS compatible fabrication procedures without additional cost. For an input power of -19.73dBm, the proposed rectifier achieves a PCE ranging from 14.68% (S=-19.73dbm, R_L=1MΩ) to 23.91% (S=-15.21dbm, R_L=0.2MΩ), and a VCE of 29.21%. Finally, for optimum implementation a careful layout and package selection must be done.

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