A 60-GHz Quadrature PLL in 90nm CMOS

F. Plessas[1], V. Panagiotopoulos[2], V. Kalenteridis[3], G. Souliotis[1], F. Liakou[1], S. Koutsomitsos[1], S. Siskos[3], A. Birbas[2]

[1] Analogies S.A., Patras, Greece, fotis.plessas@analogies.eu
[2] Dept. of Electrical & Computer Engineering, University of Patras, Greece
[3] Dept. of Physics, Aristotle University of Thessaloniki, Greece

***Abstract*—A 1.2 V 60 GHz 120 mW phase-locked loop employing a quadrature differential voltage-controlled oscillator, a programmable charge pump, and a frequency quadrupler is presented. Implemented in a 90 m CMOS process and operating at 60 GHz with a 1.2 V supply, the PLL achieves a phase noise of -91 dBc/Hz at a frequency offset of 1 MHz.**

I. INTRODUCTION

In nowadays wideband indoor or outdoor wireless systems at millimeter wave frequencies the RF local oscillator has a vital role stemming from the fact that its phase noise and frequency stability determine the sensitivity and the BER of the communication system. However in this frequency range, it is difficult to meet these requirements.

Within this context, a quadrature differential PLL tunable from 52 to 59.6 GHz with a frequency step of 50 MHz manufactured in a 90nm CMOS technology is presented, aiming at wireless transceivers in the unlicensed band from 57 to 64 GHz. The proposed architecture, shown in Fig. 1, allows the use of a lower-frequency PLL (i.e. 15 GHz) an approach which is very advantageous towards implementing a millimeter wave (i.e. 60 GHz) wide-tuning and low-phase-noise PLL [1-2].

The PLL consists of a 15 GHz quadrature differential VCO (QVCO), a programmable charge pump (CP), a high frequency divide-by-2 divider, a pulse-swallow divider including an 8/9 prescaler, a PFD, a quadrupler, a BGR, and control logic.

The QVCO is implemented by coupling two symmetric LC-tank VCOs thereby exploiting the good phase noise performance of LC-oscillators. The back-gate (body terminal) of the PMOS transistor in one VCO pair is used as the quadrature phase coupling element to the other pair.

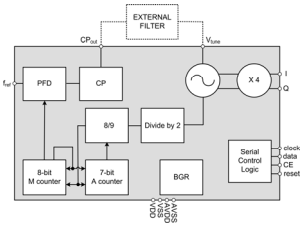

Figure 1. The proposed architecture

The programmable and accurate CP consists of four switches in a current steering configuration, a unity gain rail to rail buffer for the charge sharing effect elimination, a rail to rail amplifier for minimizing the DC output currents mismatch, a programmable current bias circuitry and two drivers based on a configuration of standard cell XOR gates for achieving good synchronization of the charge pump input pulses at the PLL lock state.

The 8/9 dual modulus prescaler is composed by a 4/5 dual modulus prescaler, a static frequency divider by 2 and a NAND gate. All circuits blocks design are based on CML logic and have been optimized in terms of speed, current consumption and silicon chip area. Also extra design effort has been dedicated to minimize phase noise contribution to the overall noise performance.

Finally, the quadrapler is a combination of a 15 to 30 GHz doubler, two 30 GHz amplifiers, a polyphase filter, a 30 to 60 GHz doubler, and two 60 GHz amplifiers.

The PLL has been designed using a 90nm CMOS process, and post layout simulation results show a phase noise of -91 dBc/Hz at 60 GHz, and a differential output swing of 70 mV at 50 Ohm while the current consumption is 100 mA at 1.2 V supply voltage. The reference spurs are 64 dB below the carrier.

II. CIRCUIT DESIGN

A. VCO

An LC CMOS cross coupled Voltage Controlled Oscillator (VCO) appears to be the most reasonable design choice for operation at the 14 GHz region. The use of both nMOS and pMOS transistors leads to better noise response. At such high frequencies varactors with extremely high tuning range have very low Q factor at the low capacitance side. This prompts to the use of a dual tuning model as in [3] employing switched capacitor arrays. The theoretical Q value of these arrays is close to the Q value of the capacitor used, while the transistor switching affects the resulting performance considerably by imposing more restraints in the on/off capacitance ratio. In this work, the need for achieving 60 GHz, leads us to a quadrature implementation. The schematic of the implemented VCO is presented in Fig. 2.

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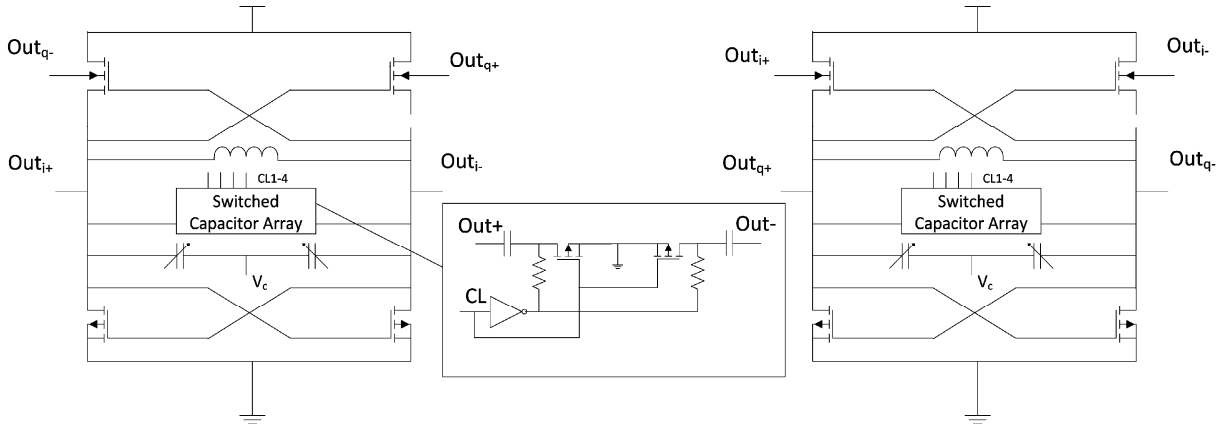

Figure 2. The schematic of the VCO

It is a typical LC CMOS cross coupled design with a switched capacitor array for coarse tuning. The varactors used are pMOS transistors on p substrates available in the process. For visual clarity the quadrature coupling network has been omitted and the ac coupling directly appears in the figure. For the quadrature signal generation two distinct differential VCOs are used in conjuction with back-gate coupling through the pMOS body. The coupling network is a capacitive network with a resistive connection to the supply, for bulk biasing. Back gate coupling, though slower in achieving the 90 degrees phase difference, has a lower impact on phase noise than coupling through transistors in parallel with the cross coupled pair. For the coarse tuning nMOS transistors are used as switches. In order to optimize the switches' behavior on both states, the internal node dc voltage is dynamically adjusted with respect to the control voltage, similarly to [4]. This allows for minimum off capacitance since the pn junction of the drain is at high reverse voltage, resulting in the least capacitance. When the nMOS is switched on, the dc operation point goes to zero achieving zero dc current and minimum on resistance.

In order to drive the quadrupler as well as the divider, a CML buffer is employed. The buffer is a two-stage design with the second stage offering dual outputs to feed both stages.

The simulations demonstrate that the VCO oscillates from 13 GHz to 14.9 GHz. The achieved phase noise at an offset of 1 MHz from the carrier is -112.5 dBc/Hz (Fig. 3). The power consumption of the core is 12.7mW.

B. Programmable Frequency Divider

The programmable frequency divider architecture based on dual-modulus prescaler is depicted in Fig. 4. The architecture consists of a dual modulus prescaler of division ratios 8 and 9 and of two programmable counters, the "S" counter and the "A" counter. The principle of operation of the divider architecture can be found in detail at [5], and it can be proven that the period of the output signal T_{out}, is expressed in terms of the input period T_{in} as follows:

$$T_{out} = (S \cdot P + A) \cdot T_{in} \quad (1)$$

where the term inside the brackets is the realized division ratio of the input signal frequency. The dual modulus prescaler 8/9, which has been utilized as a component of the programmable frequency divider is shown in Fig. 5.

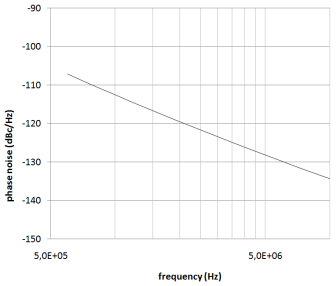

Figure 3. The phase noise of the VCO

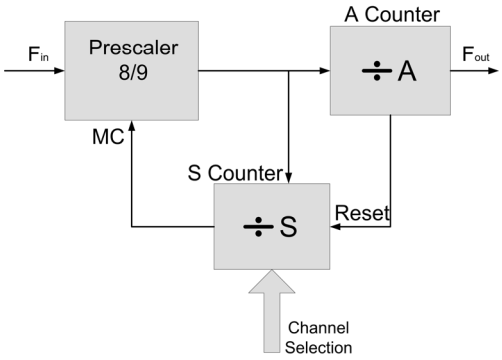

Figure 4. The programmable frequency divider

It is the most critical block of the whole architecture, since it operates at the highest frequency. It is composed by a 4/5 dual modulus prescaler, a static frequency divider of division ratio 2 and a NAND gate.

The function of the DMP prescaler 8/9 is as follows. The synchronous 4/5 DMP performs conventional divide-by-4 in the absence of a "pulse-swallow" signal. Then the output is further divided asynchronously by the static frequency divider-by-2, to generate a divide-by-8 signal. When this divide-by-8 signal, is appropriately combined with the Mod-Select signal, the third flip-flop FF3 inside the DMP 4/5 gets involved in the divider feedback loop in such a way that FF1 is forced to hold state for exactly one extra clock period. In this case a divide-by-9 ratio is obtained and the desired functionality is achieved. The design of all circuit blocks is based on CML logic and has been optimized in terms of speed, current consumption and silicon chip area.

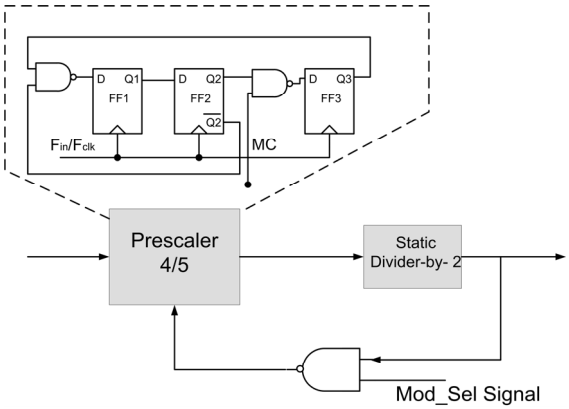

Figure 5. The dual modulus prescaler 8/9

The D-type flip-flops contain two CML latches in negative feedback configuration using polysilicon resistors as output loads instead of pmos transistors, to minimize parasitic capacitances. Since the operating frequency is half of that of the static divider, the transistor widths and the bias currents have been decreased adequately, achieving chip area and power consumption minimization. Extra design effort has been allocated to minimize the phase noise contribution to the overall noise performance.

Also a CML-to-CMOS interface circuit block is placed at the prescaler output to convert the differential CML signal to a single-ended rail-to-rail one in order to drive the CMOS logic digital counters. The specific converter design provides sufficient gain, wide bandwidth for the interest frequency range [6] and the ability of duty cycle tuning during the design phase.

C. Static Frequency Divider

A high frequency divider operating at 15 GHz with a constant division ratio of 2 has been designed in order to relax the operation of the subsequent circuit stages, in terms of speed and power consumption. Figure 6(a) shows the block diagram of the divide-by-2 static frequency divider. It is based on the typical master-slave D-type flip-flop, in which the two latches are connected in a cascaded way with negative feedback [7]. Due to its differential nature it exhibits lower switching noise and provides sufficient noise margin. As shown in Fig. 6(b) each master-slave latch is implemented using current-mode logic (CML). The master or slave part consists of the evaluation stage (M1,M2) and a latch stage (M3,M4). Transistors M5 and M6, which act as switches, are driven by the high frequency clock signal generated by the VCO circuit, steering the tail current either to M1,M2 or M3,M4 transistors, depending on the phase of the clock signal. All transistors, except from those which form the bias current mirror (M7, M8), are chosen to be low-Vt transistors, to increase the voltage margin V_{ds} of M8 and ensure its operation to the active region for all corner simulations. The aspect ratios of the drive M1, M2 and latch transistors M3, M4 are chosen to

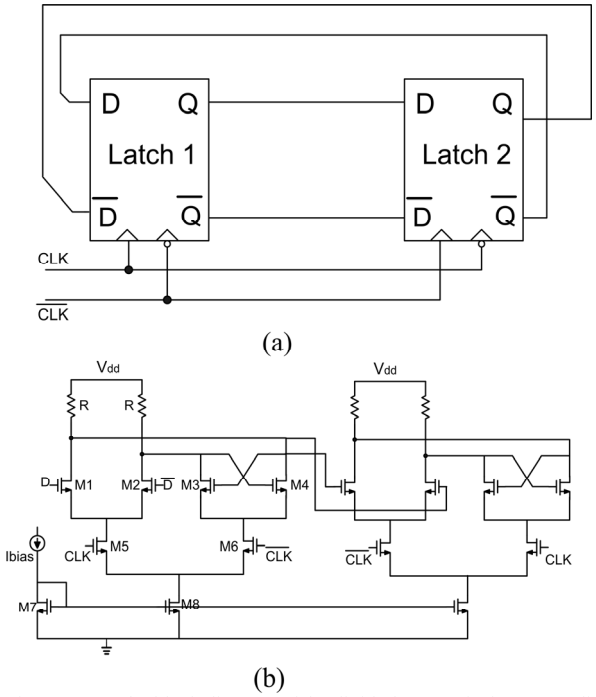

Figure 6. (a) The block diagram of the divide-by-2 static frequency divider, and (b) CML master-slave latch implementation

have a W/L ratio of 6.4μm/120nm. Clock transistor (M5, M6) dimensions are chosen to be 8μm/120nm compromising the voltage drop across them and a sufficient low gate capacitance is used to minimize the power consumption.

Polysilicon resistors are used as output loads due to their lower parasitic capacitance [8] instead of pmos transistor, to obtain higher operating frequency. Moreover, the specific type of resistor used for the design, exhibit very low dependence on technology variations, rendering more robust the operation of the divider. Also a CML clock buffer is placed before the static divider to drive adequately the clock signals generated by the VCO circuit block. Table 1 summarizes the characteristics for both circuit blocks, confirming the validation of the specifications, as they are imposed from the system level design.

D. Frequency Quadrupler

The proposed frequency quadrapler is a combination of a 15 to 30 GHz frequency doubler, two 30 GHz amplifiers, a polyphase filter, a 30 to 60 GHz frequency doubler, and two 60 GHz amplifiers as shown in Fig. 7.

Table 1

Circuit Block	Performance Characteristics			
	Operation Frequency	***Output Voltage Swing***	***Current Consumption***	***Phase Noise***
Static Divider -by-2	15GHz	100mV	2.3mA	-140dB@1MHz
Prescaler 8/9	7.5GHz	300mV	6mA	-146dB@1MHz

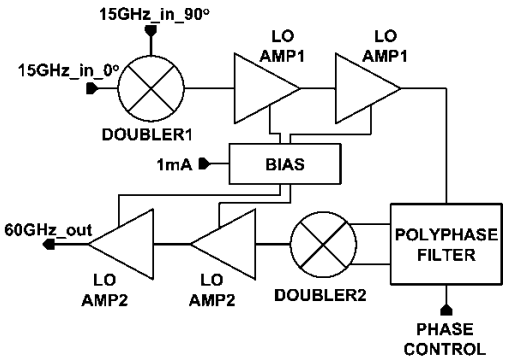

Figure 7. The frequency quadrupler

E. Phase Detector, Charge Pump and Loop Filter

A tristate phase detector has been implemented as the combination of two resettable flip-flops and an AND gate.

A programmable, accurate, highspeed, single-ended charge pump has been designed, consisting of four switches in a current steering configuration, a unity gain rail to rail buffer for eliminating the charge sharing effect, one more rail to rail amplifier for minimizing the DC current mismatch as well as a programmable current bias circuitry and two drivers based on the standard cell XOR gates specific configuration for achieving good synchronization between all charge pump input pulses at the PLL lock state. Replica biasing technique is applied to all charge pump switches. Current glitches and charge mismatch are suppressed by employing a mechanism with additional switches at the output. It exhibits a maximum DC current mismatch of 1% and charge mismatch of 6% over a wide output voltage range of 0.7V for the entire range of output currents. The wide range of the output voltage remains relatively constant and independent of the selected charge pump current amplitude. This is achieved by applying appropriate variation of the W/L ratios of the bias cascode current sources via the employment of additional programmable switches such that their saturation voltages remain relatively constant, something which in turn enables the output currents range to be as wide as it is required [9].

A second order external passive loop-filter has been employed. The components (C_1, C_2, and R_2) are optimized based on spur-suppression requirements. The RST delay is 500ps, the CP delivers a current of 200μA, and the CP charge mismatch is 10%.

III. PERFORMANCE

The proposed PLL has been fabricated in a 90 nm CMOS process. The process has eight metal layers with the top metal of 4 μm thickness. The threshold voltages of the pMOS and nMOS devices are around -0.35 V and 0.42 V, respectively. Figure 8 shows the layout view of the PLL including ESD structures and PADs. Phase noise at 1 MHz offset is -91 dBc/Hz over a tuning range from 52 to 59.6 GHz (Fig. 9). The reference spurs are 64 dB below the carrier.

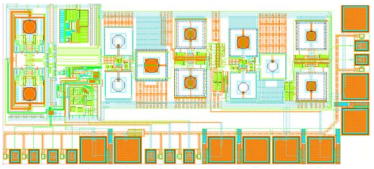

Figure 8. The layout of the 60Ghz PLL

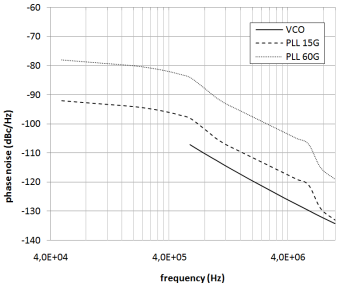

Figure 9. The total output phase noise

CONCLUSIONS

A 1.2 V 60 GHz PLL has been demonstrated, consisting of a 15 GHz quadrature differential VCO (QVCO), a programmable charge pump (CP), a high frequency divide-by-2 divider, a pulse-swallow divider including an 8/9 prescaler, a PFD, a quadrupler, a BGR, and control logic. The phase noise at 1 MHz offset is -91 dBc/Hz over a tuning range from 52 to 59.6 GHz. The total power consumption is 120mW and, the area is 2.8 mm^2 including ESDs and PADs.

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