Building blocks for a 15 GHz PLL in deep-submicron technology

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***Abstract*— In this work a 15GHz Charge Pump based PLL frequency synthesizer is presented. All circuit design has been implemented in submicron RF CMOS process with emphasis in low phase noise, low power consumption and minimum chip area. The quadrature differential VCO exhibits phase noise -112.5dBc at 1MHz offset frequency with 10.5mA current consumption. A programmable divider with a DMP 8/9 is used to achieve the desirable frequency division range. The Charge Pump features very low dc mismatch current error and is capable for low noise operation.**

Keywords- PLL, VCO, Frequency Divider, Charge Pump

I. INTRODUCTION

The wireless personal communication market has been growing explosively due to the constant introduction of new applications. Nowadays, the demand for low cost, small volume integration and long-battery life RF CMOS transceivers design for diversified wireless systems is becoming a difficult task. Among the various blocks found in such transceiver, is the frequency synthesizer which is one of the most demanding since it operates at the highest speed and a compromise between power consumption and speed has to be always satisfied [1-6].

This work focuses on the study and design of the basic building blocks of an integer-N PLL synthesizer, such as Programmable Frequency Divider, Phase-Frequency Detector (PFD), Charge Pump (CP) and Voltage-Controlled Oscillator (VCO), at both circuit and physical level for low noise and low power consumption performance. Simulation and corner analysis over PVT variations have been performed at transistor level in 90nm RF CMOS process, in order to verify their functional operation with Cadence Design Framework, but also to meet the stringent specifications imposed by the modern telecommunication systems. Moreover improved design techniques for low noise are also improvised with regards to low power and reduced die area resulting to better overall performance of the system.

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II. CIRCUIT DESCRIPTION

A. VCO

An LC CMOS quadrature cross coupled Voltage Controlled Oscillator (VCO) appears to be the most reasonable design choice for operation at the 15 GHz region. The use of both nMOS and pMOS transistors leads to better noise response. At such high frequencies varactors with extremely high tuning range have very low Q factor at the low capacitance side. This prompts to the use of a dual tuning model as in [7] employing switched capacitor arrays. The theoretical Q value of these arrays is close to the Q value of the capacitor used, while the transistor switching affects the resulting performance considerably by imposing more restraints in the on/off capacitance ratio. The schematic of the implemented VCO is presented in Fig. 1.

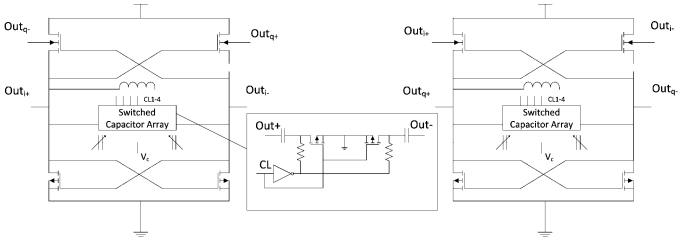

Figure 1. The schematic of the VCO

It is a typical LC CMOS cross coupled design with a switched capacitor array for coarse tuning. The varactors used are pMOS transistors on p-type substrate available in the process. For visual clarity the quadrature coupling network has been omitted and the ac coupling directly appears in the figure. For the quadrature signal generation two distinct differential VCOs are used in conjunction with back-gate coupling through the pMOS body. The coupling network is a capacitive network with a resistive connection to the supply, for bulk biasing. Back gate coupling, though slower in achieving the 90 degrees phase difference, has a lower impact on phase noise than coupling through transistors in parallel with the cross coupled pair. For the coarse tuning nMOS transistors are used as switches. In order to optimize the switches' behavior on both states, the internal node dc voltage is dynamically adjusted with respect to the control voltage, similarly to [8]. This allows for minimum off capacitance since the pn junction of the drain is at high reverse voltage, resulting in the least capacitance. When the

nMOS is switched on, the dc operation point goes to zero achieving zero dc current and minimum on resistance.
In order to drive the divider, a CML buffer is employed. The buffer is a two-stage design with the second stage offering dual outputs to feed both stages.

B. Programmable Divider

The programmable frequency divider architecture based on dual-modulus prescaler is depicted in Fig. 2. The architecture consists of a dual modulus prescaler of division ratios 8 and 9 and of two programmable counters, the "S" and the "A" counter. The principle of operation of the divider architecture can be found in detail at [9], and it can be proved that the period of the output signal T_{out}, is expressed in terms of the input period T_{in} as follows

$$T_{out}= (S\cdot P+A)\cdot T_{in} \qquad (1)$$

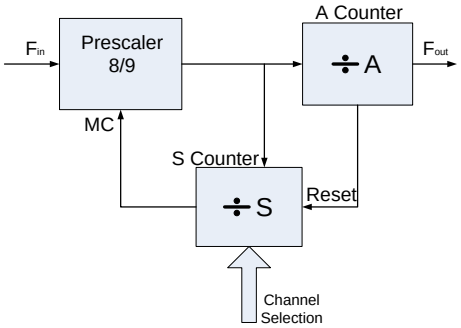

Figure 2. Programmable Frequency Divider

where the term inside the brackets is the realized division ratio of the input signal frequency.

1) Dual Modulus Prescaler 8/9

The dual modulus prescaler 8/9, which has been utilized as a component of the programmable frequency divider is shown in Fig. 3. It is the most critical block of the whole architecture, since it is operated at the highest frequency. It is individually composed by a 4/5 dual modulus prescaler, a static frequency divider of division ratio 2 and a NAND gate.

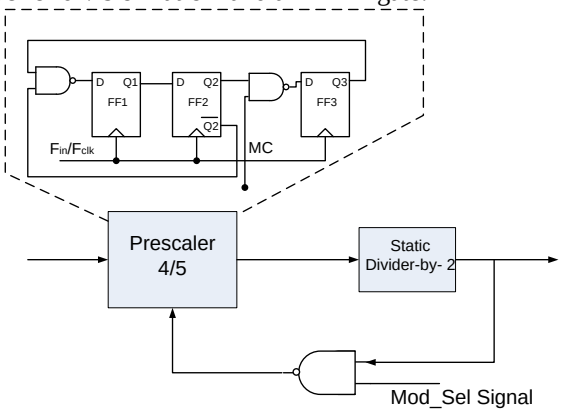

Figure 3. Dual Modulus Prescaler 8/9

The function of the DMP prescaler 8/9 is as follows. The synchronous 4/5 DMP performs conventional divide-by-4 in the absence of a "pulse-swallow" signal. Then the output is further divided asynchronously by the static frequency divider-by-2, to generate a divide-by-8 signal. When this divide-by-8 signal, is combined with the Mod-Select signal appropriately, the third flip-flop FF3 inside the DMP 4/5 gets involved in the divider feedback loop in such a way that FF1 is forced to hold state for exactly one extra clock period. In this case a divide-by-9 ratio is obtained and the appropriate functionality is achieved.

The design of all circuit blocks is based on CML logic and has been optimized in terms of speed, current consumption and silicon chip area. The D-type flip-flops contain two CML latches in negative feedback configuration with poly-resistors as output loads. Since the operating frequency is half of that of the static divider, the transistor widths and the bias currents have been decreased adequately, achieving chip area and power consumption minimization. Extra design effort has been elaborated to minimize phase noise contribution to the overall noise performance.
Also a CML-to-CMOS interface circuit block is placed at the prescaler output to convert the differential CML signal to a single-ended rail-to-rail in order to drive the CMOS logic digital counters.

2) Static Frequency Divider

A high frequency divider operating at 15 GHz with a steady division ratio 2 has been designed in order to relaxe the operation of the subsequent circuit stages, in terms of speed and power consumption. Fig.4a shows the block diagram of the divide-by-2 static frequency divider. It is based on the typical master-slave D-type flip-flop, in which the two latches are connected cascade with negative feedback [10]. Due to its differential nature it exhibits lower switching noise and provides sufficient noise margin.

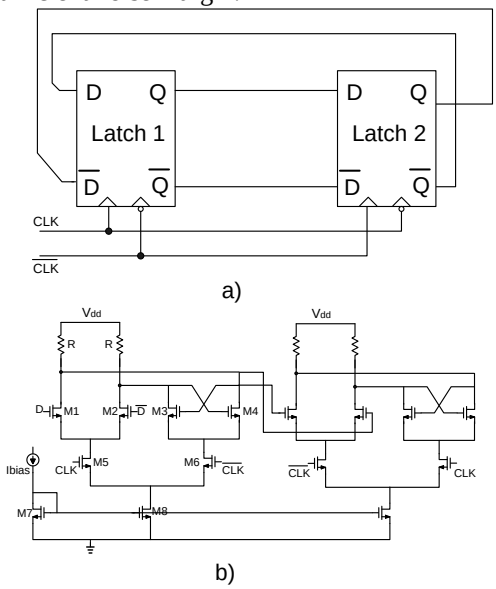

Figure 4. a) Block diagram of divide-by-2 static frequency divider, and b) CML master-slave latch implementation

As shown in Fig.4b each master-slave latch is implemented using current-mode logic (CML). The master or slave part consists of the evaluate stage (M1,M2) and a latch

stage (M3,M4). Transistor M5 and M6, which act as switches, are driven by the high frequency clock signal generated by the VCO circuit, steering the tail current either to M1,M2 or M3,M4 transistors, regards to the phase of the clock signal. All transistors, except those which form the bias current mirror (M7,M8), are chosen to be low-Vt transistors, to increase the voltage margin V_{ds} of M8 and ensure its operation to the active region for all corner simulations.

Poly-resistors are used as output loads due to their lower parasitic capacitance [10], instead of pmos transistor, to obtain higher operating frequency. Also a CML clock buffer is designed and placed before the static divider to drive adequately the clock signals generated by the VCO circuit block.

C. Charge Pump/ Phase-Frequency Detector

An accurate low-noise single-ended tri-state charge pump [11] was designed and is shown in fig. 3. This topology exhibits improved switching speed, since all nodes are precharged to the resultant operating points and current is either steered to the output, or to the unity-gain buffer. The two opamps Op1 and Op2 are used in order to minimize the DC mismatch current that could be caused by the output voltage variation.

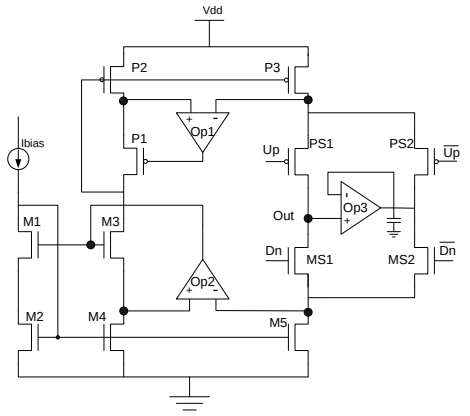

Figure 5. Low-noise Charge Pump circuit

Transistors MS1 and PS1 are the switches which are driven by the Dn and Up signals from the PFD. When the Up signal is low, PS1 switch turns on and the current Iup from P3 charges the loop filter capacitor, increasing the output voltage. On the other hand when the Dn signal is high, MS1 switch is turned on and the output voltage is decreased by the discharging current Idn that flows through M5. When the loop is locked, both switches are on for a small fraction of time. At this condition, the switches have to be turned on and off at the same time, in order to avoid extra noise contribution from the devices to the output of the circuit. Moreover the unity gain amplifier Op3 plays an important role, since it sets the voltage at the drain of the switches PS1 and MS1 at the output node. Thus the charge sharing effect becomes marginal when the switches turned on. It also increases the switching-speed of the charge pump due to current constant flow from P3 to M5, even when the PLL is locked. The significant improvement compared to similar, alternative charge pump implementations [3-4] is in essence due to the fact that the output of the opamps drives the gates of the cascode transistors and not directly the gates of the current source transistors.

The Phase-Frequency Detector, depicted in figure 6, in the dashed cycle, consists of two positive edge-triggered D flip-flops and a delayed feedback path containing a NAND gate and a number of inverters. These inverters create a delay, which prevents the dead-zone problem, when the PLL is in locked condition. A timing synchronization scheme which constitute from two buffer chains, one for the Up signal and another for the Dn signal, is placed between PFD and CP, as shown in the same figure. The scaling ratio for the inverters is chosen to be close to 4 [12], in order to obtain the best trade-off for power, speed and area. Also the channel length L, of nMOS transistor of the first inverter of the Up signal is increased to equalize the delay between the two timing control signals.

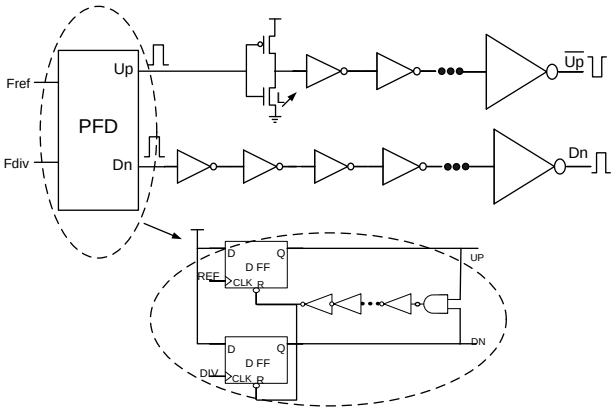

Figure 6. Phase-Frequency Detector and CMOS Buffer Chain

III. SIMULATION RESULTS

VCO, Static frequency divider and Prescaler 8/9 were designed and integrated in 90nm RF CMOS technology with 1.2V supply voltage. Simulation results obtained by SpectreRF indicate that the VCO oscillates from 13 GHz to 14.9 GHz. The achieved phase noise at an offset of 1 MHz from the carrier is -112.5 dBc/Hz (Fig. 7). The power consumption of the core is 12.7mW.

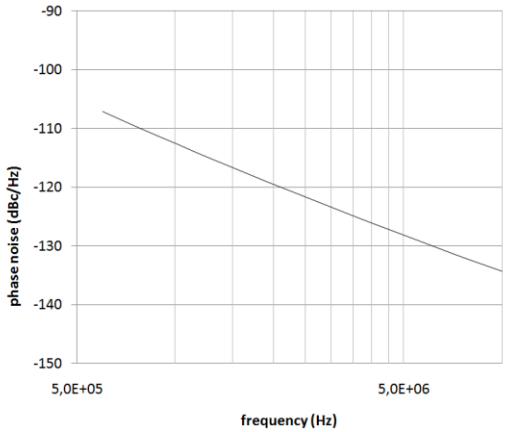

Figure 7. VCO Phase Noise

Table I summarizes the characteristics for Static frequency divider and Prescaler 8/9, confirming the achievement of the

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TABLE I. PERFORMANCE CHARACTERISTICS

Circuit	Performance Parameters		
	Operation frequency	***Output Voltage Swing***	***Phase Noise(dB)***
Static Divider	15GHz	100mV	-140@1MHz
Prescaler 8/9	7.5GHz	300mV	-146@1MHz

system level specifications. The above results are obtained at typical conditions (0-σ@27^{o}C). It should be noted that the Static divider consumes 2.3mA and is capable of operation up to 17GHz under process, temperature and voltage supply variations, with extra current consumption. Moreover DMP 8/9 current consumption is 6mA at 7.5GHz operation frequency.

The proposed charge pump was designed using 180nm CMOS RF technology. The supply voltage was 2.5Volt for the charge pump and inverters in the buffer chain. The pump up and pump down currents are 1mA from a 2.5V power supply. The percentage of DC mismatch current over output voltage of the proposed CP, for three different corners (typical, slow, fast) and temperature cases (27C, 85C, -45C), is shown in fig. 8.

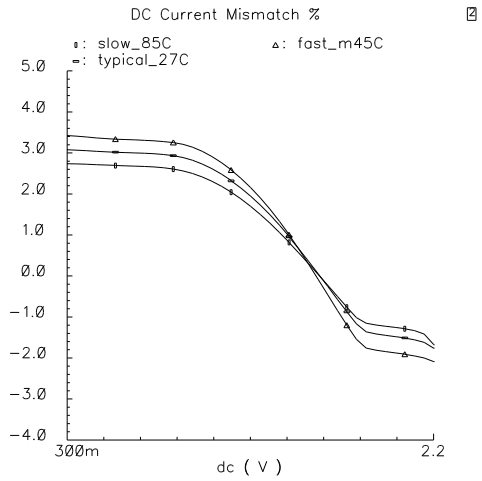

Figure 8. DC mismatch of the output current

The circuit is able to operate with a mismatch current less than ±2.25% at the typical case and 2.5% at the slow-hot. The output voltage ranges from 300mV to 2.2V. Beyond these limits, transistors close to the supply rails (P3, M5), turn from the saturation and enter to the linear region of operation which results to an increase of the mismatch current. In addition the charge pump can achieve a dead-zone time response of 500ps, minimizing the overall noise performance of the loop.

IV. CONCLUSIONS

In this paper an abstract description of the essential building blocks integrated in a 15GHz PLL frequency synthesizer has been done. Critical design parameters such as VCO phase noise or Charge Pump noise contribution have been optimized in order to meet the system level specifications. Static Frequency Divider and Dual Modulus Prescaler 8/9 perfromance characteristics, such as operation frequency, phase noise and voltage swing are in agreement with the initial design specifications.

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