A variable gain wideband CMOS low-noise amplifier for 75 MHz - 3 GHz wireless receivers

Chrysoula Vassou[1], Fotis Plessas[2], Nikolaos Terzopoulos[3]
[1]Department of Physics, Aristotle University of Thessaloniki, Greece
[2]Department of Electrical and Computer Engineering, University of Thessaly, Greece
[3]Department of Computing & Communication Technologies, Faculty of Technology, Design & Environment, Oxford Brookes University, Wheatley, Oxford, UK

***Abstract*—A wideband CMOS variable gain low noise amplifier suitable for multi-standard radio applications between 75 MHz and 3 GHz is presented. Wideband matching to 50 Ohm (single ended) is achieved using a common-drain feedback stage whereas variable gain is realized using a resistive attenuator. The circuit has been designed in a 65 nm CMOS process and achieves 22 dB maximum gain, 29 dB gain range, 3.3 dB noise figure, and an IIP3 higher than -4 dBm.**

I. INTRODUCTION

Many different Wireless Communication Standards have been introduced the past few decades to facilitate the increasing end user's demands. These standards can be grouped in three major categories: voice and moderate-speed data communication needs fulfilled by the cellular access technologies such as GSM and CDMA, high data rate demand mainly satisfied by the IEEE 802.11 series of standards and finally, the need of establishing a Private-Area Network (PAN)is made possible via the introduction of the Bluetooth standard. Furthermore, satellite based positioning systems (for e.g. GPS, GLONASS, Galileo) operate also at nearby frequencies and there are several standards available worldwide for the Digital Television (DTV) application using a number of different frequency bands [1].

The aforementioned user demands places a great number of design challenges considering the development of the LNA as being the most critical block of an analog front end. The LNA circuit designer has to take key considerations into account, the most important being the ability to operate across a wide range of frequencies, followed by sufficient gain in order to overcome noise contribution by subsequent stages. Apart from that, the gain should remain as flat as possible within the specified range of frequencies (bandwidth) to avoid distortions. The LNA must also provide good handling of large signals without distortions, i.e. has good linearity. In addition, as the antenna is commonly designed for the standard 50 Ohm termination, the input impedance of the LNA must he matched to 50 Ohm to ensure optimum power transfer.

Most commonly used methods to achieve multiband/wideband functionality include the use of either a number of frequency selective type of LNAs connected in parallel or a switching output load [2-4]. While the main drawback of this approach is the large die area early versions of wideband amplifiers such as the shunt-series feedback amplifier and the common-gate amplifier suffers from poor noise figure and do require the input impedance to be matched [5].

Single-ended input LNAs are usually preferred to minimize the use of I/O pins and also due to the fact that antennas and RF filters produce a single ended signal. In contrast, on the receiver side, differential signaling is preferred for reducing the second-order distortion while rejecting power supply and substrate noise.

Regarding gain programmability, the available LNA design approaches are limited to either a non-programmable topology complying with all recommended specifications simultaneously or as a programmable topology conforming in

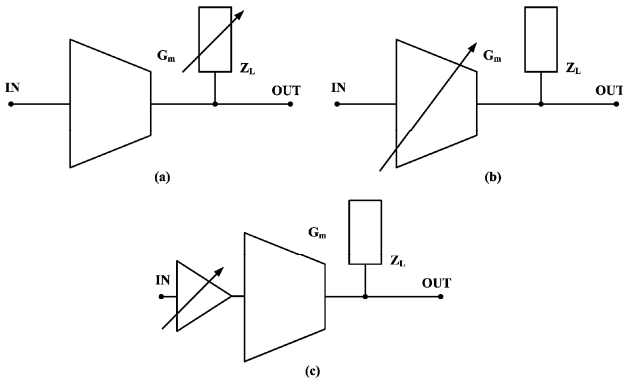

Fig. 1 Configurable-gain topologies

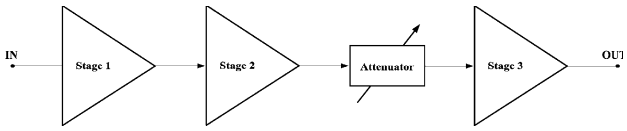

Fig. 2 Block diagram of the two stage wideband variable gain LNA

this way to a variety of different set of specifications and input power ranges.

Typically, the programmable LNA architectures are usually developed by varying either the load impedance [6], [7], the input transconductance [8]–[10], or using pre-attenuation-based topologies [11]–[15], as shown in Fig. 1.

In this paper, we are going to present the design of a variable gain LNA capable of simultaneous operation in the band ranging from 75 MHz to 3 GHz on a well-established commercial digital 65 nm CMOS process as shown in Fig. 2. In order to achieve a wideband impedance-matching to 50 Ohm (single ended) we make use of a common-drain feedback stage, while the variable-gain functionality is implemented using an attenuator. Each individual block will be thoroughly investigated in later sections, along with the performance of the LNA.

II. Circuit Design

A. Stage 1

The input stage is a common-source amplifier with a common-drain feedback stage, as shown in Fig. 3 [16].

A differential topology has been selected as it is well-known for being robust and less sensistive to supply noise. The cascode transistor M2 is used to reduce the Miller effect and to improve the reverse isolation. The wideband impedance-matching of 50 Ohm (single ended) is achieved by using a common-drain feedback stage consisting of M4 and R2. Transistor M5 along with the resistor R4 acting as a current source. The selected architecture provides additional flexibility when used for low noise figure performance

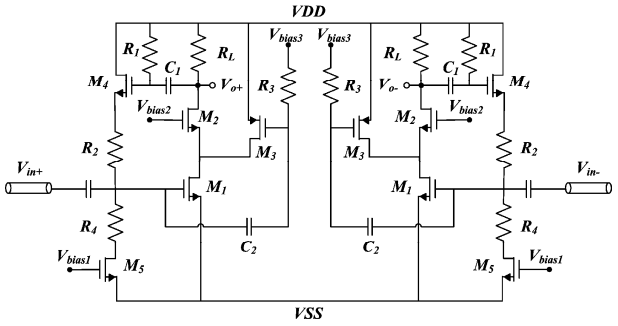

Fig. 3 Stage 1 (input stage) of the proposed wideband LNA

(dependent mainly on M1) while at the same time meets the required input impedance specification (controlled by M4).

To ensure a certain tranconductance level and to maintain an adequate linerity, a quite large, dimensions wise, input transistor is needed along with a certain amount of bias current. Thus, the cascode transistor is driven into the linear region due to the reduced headroom caused by a voltage drop at the resistive load R_L. Minimizing the resistance R_L is not an available option since that would cause a gain drop. Although the proposed LNA operates at an I/O voltage of 2.5V, for an implementation in 65 nm CMOS process with a core supply voltage of 1.2 V the voltage drop would have been too large and therefore the PMOS transistor (M3) is inserted. The purpose of this transistor is mainly to feed a bias current to the main input transistor (M1) ensuring that not all of the current has to flow through the load resistor and the cascode transistor (M2).

By connecting the gate of M3 to the input the overall gain will be improved, even though the transconductance of the M3 is smaller in comparison with that of M1,while the noise contribution will be reduced.

The gain of the input stage is:

$$A_v = -\left(g_{m,M1} + g_{m,M3}\right) R_L \frac{g_{m,M2}}{g_{m,M2} + g_{ds,M1} + g_{ds,M3}} \quad (1)$$

The wideband impedance matching to the source impedance is provided by the common-drain feedback stage, consisting of M4 and R2. The feedback transistor M4 is AC-coupled in order to be biased independently of the output's DC-level. The LNA's output drives the gate of M4 with a signal of large voltage amplitude. This large signal-swing at the output leads to a non-linear response from the feedback path with immediate effect to the linearity of the entire LNA. To rectify this undesired behavior, the resistor (R2) is connected in series with the M4 to improve the linearity of the feedback mechanism.

Ignoring the reactances, the input impedance can be expressed as:

$$Z_{in} = \frac{1 + g_{m,M4} R_2}{g_{m,M4}(1 + |A_v|)} \quad (2)$$

Concerning the noise figure, all transistors and resistors are assumed to generate a noise voltage appearing at the output. A significanlty downscaled and bandlimited version of this noise is fed back to the input through the common-drain feedback stage, where it gets amplified and inverted before coming out at the output. This feedback mechanism cancels some of the correlated noise and thus, the overall output noise is reduced. All resistors and transistors, except M5, are part of this feedback loop and their noise contribution is partialy cancelled. The noise from M5 appears directly at the input and since this transistor is outside the feedback loop its noise contribution is amplified and summed at the output. To avoid this unseccary contribution, it is important to keep $g_{m,M5}$ as small as possible. This can be done since $g_{m,M5}$ has nothing to do with neither gain or input impedance.

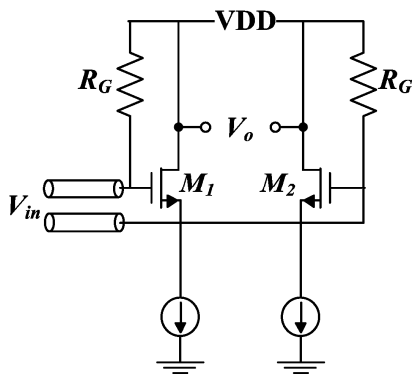

Fig. 4 The buffer employed in Stages 2 and 3

B. Stage 2and Stage 3

The buffer, shown in Fig 4. is implemented as two common-drain stages.

The main purpose of using these stages is to accomplish a differential output impedance of 600 Ohm. In order to reduce the parasitic capacitance at the input of the buffer, the sizes of M1 and M2 (Fig. 4) should be kept at a minimum possible, despite the higher loss being equal to 2 dB for each one.

C. Attenuator

The resistor based attenuator has excellent linearity and accounts for less area, whereas impedance matching can be easily achieved. Fig. 5 shows the proposed attenuator with five gain steps.

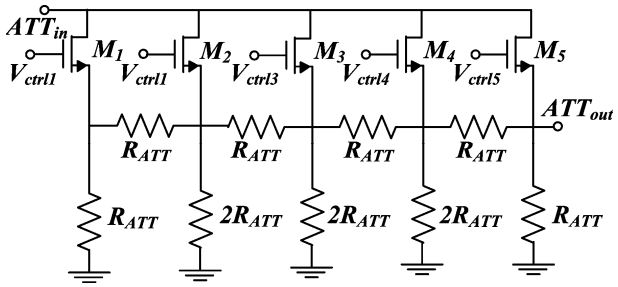

Fig. 5 The attenuator (single ended version shown)

Attenuation is realized by controlling the NMOS switches. When one of the switches is on, the impedance seen from ATTin is a constant, given as:

$$R_{in} = 2/3R_{ATT} \quad (3)$$

If the output impedance of the 2nd stage is 300 Ohm (single ended), the value for R_{ATT} in Fig.5 can be calculated to be 450 Ohm.

III. PERFORMANCE

This section presents the simulation results for the proposed LNA. Voltage gain, noise figure, IIP3, and results over frequency are presented for all cases.

The proposed LNA achieves a total voltage gain range of 29 dB, with a maximum voltage gain of 22 dB and a minimum gain of -7 dB, as shown in Fig. 6. The S_{11} is below -9 dB along the bandwidth (75 MHz – 3.0 GHz) in all operating modes, as shown in Fig. 7. The IIP3 has an almost flat frequency response with a minimum value (at 22 dB gain) higher than -4 dBm at 2 GHz. The noise figure has a minimum value of 3.3 dB at the maximum-gain setting, as can be seen in Fig. 8. Finally, the LNA is unconditionally stable across the full band range while the input impedance can be easily adjusted to 75 Ohm by modifying appropriately the feedback path.

A comparison with other, recently published, alternative configurable amplifier topologies covering the same frequency range is shown in Table I. In [17], a wideband LNA with gain control and current reuse is designed, providing a 13 dB max gain from 470 MHz to 3 GHz whereas, in [18], a wideband, inductorless architecture with one gain step of ~28 dB is proposed. In [19] a programmable wideband LNA for the Gigabit Home Networking (G.hn) wired technology is presented operating at frequencies ranging from 300 MHz to 2.5 GHz.

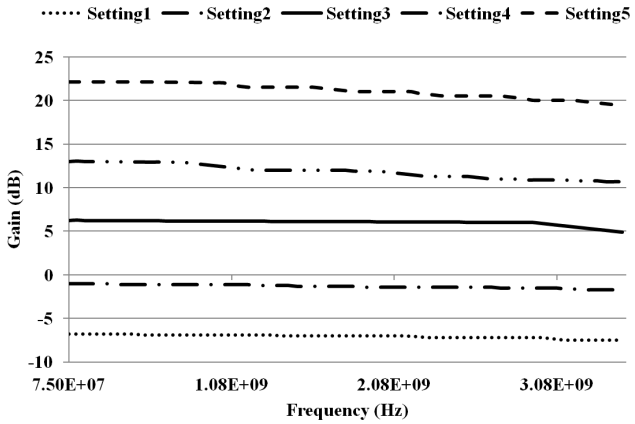

Fig. 6 Voltage gain simulation results

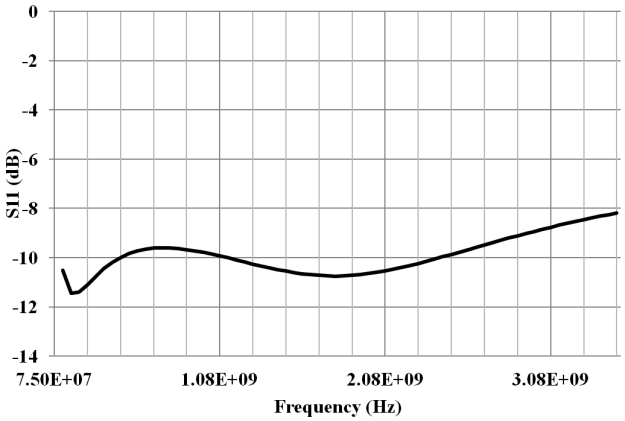

Fig. 7 S_{11} simulation results (for all settings)

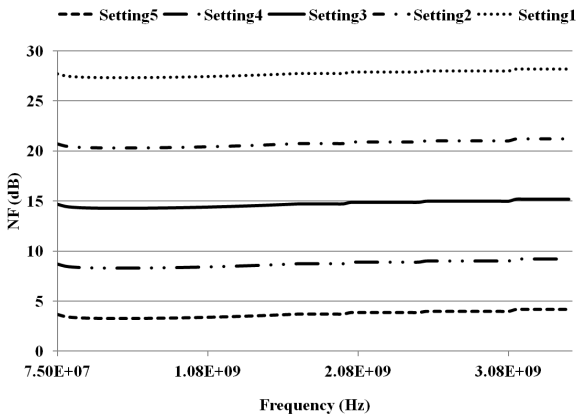

Fig. 8 NF simulation results

TABLE I. PERFORMANCE COMPARISON

Ref	[17]	[18]	[19]	This work
Bandwidth (GHz)	0.47~3.0	0.01~5.0	0.3~2.5	0.075-3
Voltage gain (dB)	7~13	-10 or +18 (one gain step)	-16.6~13.4	-7~22
Min. NF (dB)	2.5	2	3.2	3.3
IIP3 (dBm)	-3.5	-10 (max 20)	-1.8 (max 28.9)	-4
Power (mW)	5.4~27	2 or 38	23~24.3	16.5
Inductorless	No	Yes	Yes	Yes
Differential	No	No	Yes	Yes
Process	180nm	90nm	65nm	65nm

It should be noted that most of the tabular data in Table I are measurement results, but in our case the reported findings are based on corner simulations (slow-slow, 2.25V, -40°C).

IV. CONCLUSIONS

In this paper, a CMOS wideband, variable gain, inductorless, fully differential low noise amplifier is presented. To provide wideband matching to 50 Ohm (single ended) for the LNA, a common-drain feedback stage has been proposed. Also, a gain control block employing a resistive attenuator has been implemented. Its performance is directly comparable to recent publications for applications like WiFi, WiMax, Bluetooth etc providing a gain of 22 dB, a gain range of 29 dB, good input matching (S11<-9dB), a minimum noise figure of 3.3 dB, and an IIP3 of -4 dBm, while it only draws 6.6 mA from a 2.5 V supply.

REFERENCES

[1] Report ITU-R M.2024(2000), "Summary of spectrum usage survey results". Available: http://www.itu.int/pub/R-REP-M.2024-2000 [Accessed 8 Sep 2013].

[2] Ying-Che Chung, Chih-Wei Chen, Oscal T.-C. Chen, Robert Y.J. Tsen, "A multi-band RF front-end receiver for Bluetooth, WCDMA, and GPS applications," 2003 IEEE 46th Midwest Symposium on Circuits and Systems,Cairo, Egypt, pp. 1175 – 1178.

[3] Rahul Magoon, Alyosha Molnar, Jeff Zachan, Geoff Hatcher, and Woogeun Rhee, "A Single-Chip Quad-Band (850/900/1800/1900 MHz) Direct Conversion GSM/GPRS RF Transceiver with Integrated VCOs and Fractional-N Synthesizer," IEEE J. Solid-State Circuits, vol. 37, no. 12, pp. 1710-1720, Dec. 2002.

[4] Vu Kien Dao, Quang Diep Bui and Chul Soon Park, "A Multi-band 900MHz/1.8GHz/5.2GHz LNA for Reconfigurable Radio," 2007 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Honolulu, USA, pp. 69-72, June 2007.

[5] F. Bruccoleri, E.A.M. Klumperink, B. Nauta, "Noise cancelling in wideband CMOS LNAs," in 2002 IEEE Solid-State Circuits Conference. Digest of Technical Papers (ISSCC 2002), Feb. 2002, San Francisco, USA, pp. 406 – 407.

[6] M. Dawkins, A. Burdett, and N. Cowley, "A single-chip tuner for DVB-T," IEEE J. Solid-State Circuits, vol. 38, no. 8, pp. 1307–1317, Aug. 2003.

[7] L. Connell, N. Hollenbeck, M. Bushman, B. McCarthy, S. Bergstedt, R. Cieslak, and J. Caldwell, "A CMOS broadband tuner IC," in IEEE Int. Solid-State Circuits Conf. Tech. Dig., 2002, vol. 2, pp. 324–529.

[8] P. Antoine, P. Bauser, H. Beaulaton,M. Buchholz, D. Carey, T. Cassagnes, T. Chan, S. Colomines, F. Hurley, D. Jobling, N. Kearney, A. Murphy, J. Rock, D. Salle, and C.-T. Tu, "A direct-conversion receiver for DVB-H," in IEEE Int. Solid-State Circuits Conf. Tech. Dig., Feb. 2005, vol. 1, pp. 426–607.

[9] H. Riihihuhta, K. Halonen, and K. Koli, "A high dynamic range 100 MHz AGC-amplifier with a linear and temperature compensated gain control," in IEEE Int. Circuits Syst. Symp., May 1994, vol. 5, pp. 521–524, vol. 5.

[10] Y. Takamatsu, R. Fujimoto, T. Yasuda, T. Sekine, T. Hirakawa, M. Ishii, M. Hayashi, and N. Itoh, "A tunable low-noise amplifier for digital TV applications," in IEEE Asian Solid-State Circuits Conf., Nov. 2009, pp. 273–276.

[11] D. Im, H.-T. Kim, and K. Lee, "A CMOS resistive feedback differential low-noise amplifier with enhanced loop gain for digital TV tuner applications," IEEE Trans. Microw. Theory Tech., vol. 57, no. 11, pp. 2633–2642, Nov. 2009.

[12] K. Iizuka, H. Kawamura, T. Fujiwara, K. Kagoshima, S. Kawama, H. Kijima, M. Koutani, S. Toyoyama, and K. Sakuno, "A 184mW fully integrated DVB-H tuner with a linearized variable gain LNA and quadrature mixers using cross-coupled transconductor," IEEE J. Solid-State Circuits, vol. 42, no. 4, pp. 862–871, Apr. 2007.

[13] M. Koutani, H. Kawamura, S. Toyoyama, and K. Iizuka, "A digitally controlled variable-gain low-noise amplifier with strong immunity to interferers," IEEE J. Solid-State Circuits, vol. 42, no. 11, pp. 2395–2403, Nov. 2007.

[14] I. Mehr, S. Rose, S. Nesterenko, D. Paterson, R. Schreier, H. L'Bahy, S. Kidambi, M. Elliott, and S. Puckett, "A dual-conversion tuner for multi-standard terrestrial and cable reception," in VLSI Circuits Symp. Tech. Dig., Jun. 2005, pp. 340–343.

[15] J. Xiao, I. Mehr, and J. Silva-Martinez, "A high dynamic range CMOS variable gain amplifier formobile DTV tuner," IEEE J. Solid-State Circuits, vol. 42, no. 2, pp. 292–301, Feb. 2007.

[16] R. Ramzan, S. Andersson, J. Dabrowski, C. Svensson, "A 1.4V 25mW Inductorless Wideband LNA in 0.13µm CMOS," in IEEE International Solid-State Circuits Conference. Digest of Technical Papers (ISSCC 2007), Feb. 2007, San Francisco, CA, USA, pp. 424–613.

[17] San-Fu Wang, Yuh-Shyan Hwang, Shou-Chung Yan, Jiann-Jong Chen, "A new CMOS wideband low noise amplifier with gain control," Integration, the VLSI journal, vol. 44, no. 2, pp. 136-143, Mar. 2011.

[18] Jing-Hong Conan Zhan, Stewart S. Taylor, "An Inductor-Less Broadband LNA with Gain Step," in 32nd European Solid-State Circuits Conference (ESSCIRC 2006), Sep 2006, Montreux, Switzerland, pp. 344-347.

[19] Xavier Trulls, Diego Mateo, and Adria Bofill, "A High Dynamic-Range RF Programmable-Gain Front End for G.hn RF-Coax in 65-nm CMOS," IEEE Trans. Microw. Theory Tech., vol. 60, no. 10, pp. 3243–3253, Oct. 2012.