A 16-GHz Differential LC-VCO in 16-nm CMOS

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Abstract

In this paper, a 16-GHz , 16nm CMOS differential Voltage Controlled Oscillator(VCO) is presented. Filtering is used at the common source node of the cross-coupled transistors to effectively lower phase noise contributors. The oscillator has been implemented using 16nm Predictive Technology Models(PTMs) [1], which achieve -89.210dBc/Hz at 1MHz offset, drawing 12.7mA from a 0.9-V supply.

Keywords - Differential VCO, CMOS, Phase Noise, Source Filtering.

1 Introduction

In recent days, due to the immense growth of both wireless and optical communications systems, low-phase noise high frequency oscillator units have become a necessity. Local oscillators, with as low as possible phase noise, are needed in Radio Frequency(RF) transceivers, where the information signal is modulated or demodulated. During this process the bit-error-rate(BER) characteristic is highly dependent of the phase noise added by the VCO. Although Ring Oscillators are really simple and attractive topologies, from the standpoint of circuit integration, LC oscillators are the only means in achieving really good phase noise performance. The differential cross-coupled LC oscillator is well known for its good phase noise characteristics and thus is implemented in this paper [2]. According to the measurements, the circuit is capable of producing low-phase noise signals, with a power consumption of almost 11.43mW, that could be used in any CMOS transceiver of the previously mentioned frequency.

2 Circuit Design

The schematic of the differential LC-oscillator is shown in Fig. 1. The main core of the oscillator consists of two cross-coupled nMos transistors and the LC-tank. Furthermore, we have implemented a simple current mirror, with a capacitor in parallel, that provides the circuit with the demanded current through a source inductor.

The two cross-coupled transistors are responsible to provide the negative resistance, amplifier stage, which in turn compensates for the resonator losses and at the same time stabilizes the oscillation.

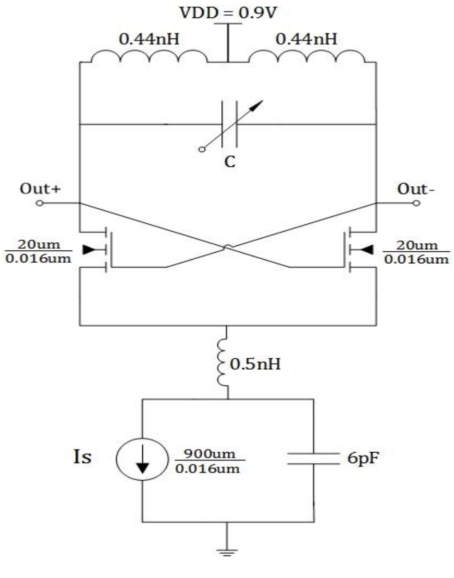

Fig. 1. VCO Schematic

The resonator, in essence the LC-tank, consists of inductors and varactors which are also responsible for stabilizing the oscillation around our center frequency, f_o. Excluding the circuit's active elements, the passive elements constituting the resonator (inductors, varactors) are dominating the phase noise characteristics of our design and further degrade its performance. To reduce the noise lossy inductors impose to our circuit, inductors with higher quality factors(Q) should be implemented leading to lower resistive loss and subsequently lower noise and power dissipation. However, the quality factor is limited by the integration technology and there is not much the designer could do towards this direction.

In order to provide the desirable frequency fine-tuning in our design varactors are used. The overall phase noise performance of our LC-VCO is significantly affected by the design and modeling of the varactor. MOS-based Inversion type varactors were used due to their high Q-factor, wide tuning range, which improve with every new process generation, and implementation simplicity [3]. A pMOS-varactor has the same structure as a pMOS transistor, with its gate as the first terminal and drain-source as the second while the bulk is connected directly to V_{DD}. In Fig. 2.A we present the exact connection and the capacitance over the tuning range characteristic follows in Fig. 2.B.

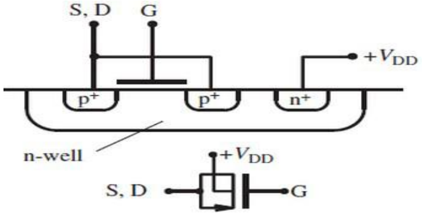

Fig. 2.A MOS Inversion type Varactor Cross-section & Connection

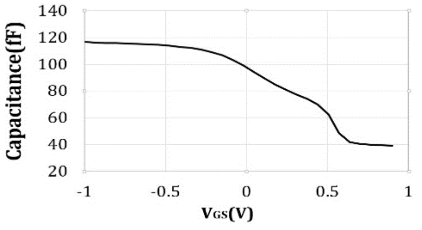

Fig. 2.B Capacitance – V_{GS} Curve

Furthermore, several stages of the previously mentioned structure in parallel can be utilized in order to provide the specific capacitance needed for our center frequency oscillation.

Still, the C-V characteristics of a pMOS varactor could not be easily modeled. Although we know the oscillation frequency of an oscillator is computed using equation (1).

$$f_o = \frac{1}{2\pi\sqrt{L \cdot C(V)}}, (1)$$

where L is the inductance and C(V) is the equivalent capacitance at a given biasing point.

Simply solving equation (1), we could get the norm to model C(V) given a certain oscillation frequency and inductance as presented in equation (2).

$$C(V) = \frac{1}{4\pi^2 \cdot f_o^2 \cdot L}, (2)$$

Apart from all the preceding, it is critical to take into account that capacitance is dependent not only on the signal swing of the output but also on the contribution of the center frequency harmonics.

In addition, the source inductor with the current mirror and the capacitor connected in parallel form a filtered current source, which improves significantly the phase-noise performance of the oscillator. Although, we would prefer the current source to be ideally noiseless and have a high impedance at $2f_o$(second harmonic frequency) to prevent the cross coupled pair from loading the resonator, this is not easily achieved.

A source inductor is therefore used to resonate the parasitics of the current source at $2f_o$ and the parallel capacitor reduces the high-frequency noise contribution of the current source providing path to ground [4]-[6]. So, to summarize this filtering technique prevents tail current noise at $2f_o$-using the source inductor- and reduces high-frequency noise-using the parallel capacitor. We have to also take into account the low-frequency tail current noise, which converts into phase-noise and is caused by the non-ideal behavior of the current source. To enable measurements the oscillator output drives 100Ω loads.

3 Phase Noise Improvement Techniques

Some of the most important phase noise contributors are, the noise the tail current source feeds the circuit around the second harmonic frequency($2f_o$), the noise due to the resistance of the cross-coupled transistors and the in-band noise of the LC-tank. The most difficult challenge in oscillator design is to simultaneously achieve low phase noise performance minimizing the contribution of the previously mentioned factors and at the same time meet or even better exceed the oscillator specifications.
In the following paragraphs we will outline some of the most commonly used techniques in order to minimize phase noise and the effects induced in our circuit design.
1. A High Quality Factor(Q) Resonator

In LC oscillator topologies the quality factor of the resonator is one of the most important design variables. We already know that the Q-factor of every LC-tank is constrained by the inductor's Q, given that inductors present a higher degree of energy dissipation as compared to capacitors. The dependence of phase noise to the resonator's quality factor can be attained from Leeson's formula, presented in equation (3).

$$L(f_m) = 10\log[\,\tfrac{1}{2}((\frac{f_o}{2\cdot Q\cdot f_m})^2 + 1)(\frac{f_c}{f_m} + 1)(\frac{FkT}{P})\,], \quad (3)$$

where f_o is the output frequency, Q is the resonator Q, f_m is the offset from the output frequency(Hz), f_c is the 1/f corner frequency, F is the noise factor of the amplifier, k is Boltzmann's constant, T is absolute temperature in Kelvins, and P is the oscillator output power.
Hence, a high Q-factor inductor would provide an LC-tank which would work as a very effective band-pass filter around our center frequency cutting off as many as possible noise components -ideally all. Furthermore, a high Q-factor indicates less LC-tank in-band noise and significantly bounds its losses, leading to much better phase noise performance and decreased power requirements to maintain oscillation. This method is the most efficient as compared to other techniques but is highly dependent on the integration technology dimensions, in our case 16nm. The simulated results presented in Tab. 1. prove that even a small improvement in the Q-factor can significantly affect phase noise. Our topology's enhancement reached over 2dBc with almost the same power consumption.

Q	Power(mW)	PN@1MHz(dBc/Hz)
6	6.9	-83.395
12	7.03	-85.757

Tab. 1. Quality factor Contribution to Phase Noise

2. Increase Tail Current

Phase noise is the measure of purity of a local oscillator and its most critical specification. Since it is calculated as the ratio of noise power to output signal power in a 1Hz bandwidth at a given offset from the carrier signal, providing a larger signal to our circuit would improve phase noise. The easiest way to to achieve a greater signal is by providing the circuit with higher tail current. However, better phase noise due to increased tail current comes at the expense of higher power dissipation, which is not always feasible. Furthermore, if the cross-coupled transistors have reached their saturation limit, no matter how much current is provided to the circuit, its output will remain unaffected. These are the main reasons this technique should be implemented with caution, bearing in mind that increased tail current induces further noise to the circuit, due to the non-ideal current source, and greater power consumption. In Tab. 2. we have gathered some simulation measurements with regard to tail current and it is easily concluded that small increases in the current supplying our circuit can result to much better overall phase noise performance.

I_{tail}(mA)	Freq(GHz)	PN@1MHz(dBc/Hz)
12.7	16	-86.708
8.75	16	-83.898
5.82	15.96	-79.943
5.07	15.96	-76.054

Tab. 2. Tail Current Contribution to Phase Noise

3. Current Source Filtering

A current source with almost ideal, noiseless, behavior is not easily achieved and all the non-linearities that stem from this phenomenon are converted in phase noise. In an effort to reduce these contributions a large capacitor is connected in parallel with the current source and shunts the high-frequency noise to the ground. In addition, to provide high impedance and at the same time resonate the parasitics of the current source at the second harmonic($2f_o$) a source inductor is implemented connecting the current source with the cross-coupled transistors. The simulation results provided in Tab. 3. show that for the exact same design and power consumption, source filtering exhibits much better phase noise characteristics and should be therefore implemented wherever design constraints permit it.

Source Filtering	Freq(GHz)	I_{tail}(mA)	PN@1MHz (dBc/Hz)
Without	15.97	12.6	-76.575
With	16	12.7	-86.708
Without	16.06	11.6	-77.467
With	16.08	11.5	-85.753
Without	15.99	8.76	-82.444
With	16	8.75	-83.898

Tab. 3. Current Source Filtering Contribution to Phase Noise

4 Results & Conclusions

The improvement current source filtering provided to our circuit is not negligible and can be observed in Fig. 3. since the phase-noise performance at 1MHz offset from f_o is -89.210dBc/Hz for the source-filtered implementation while only -76.58dBc/Hz for the current source without inductive filtering.

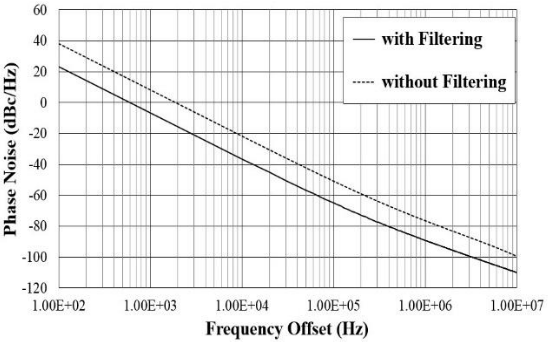

Fig. 3. Phase Noise performance, with and without Source Filtering

Furthermore, the output frequency ranges from 15.6 to 16.6 GHz with control voltages varying from 0.15 to 0.9V. The center frequency of the implemented VCO, f_o, is 16GHz and the differential Voltage output in dBm, is 2.531 driving 100Ω loads at its output.

It is also critical to observe the severe attenuation at the second harmonic due to $2f_o$ filtering, as presented in Fig. 4., which also improved phase noise.

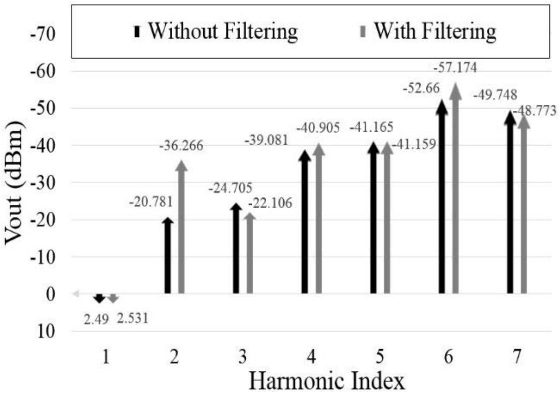

Fig. 4. Harmonic Amplitude in dBm, with and without Source Filtering

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