A 16-nm FinFET 16-GHz Differential LC-VCO

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***Abstract*- In this paper, a 16-GHz FinFET differential Voltage-Controlled Oscillator (VCO) is presented. Filtering is used at the common source node of the cross-coupled transistors as well as other techniques to effectively lower phase noise. The oscillator is designed using 16nm FinFET Predictive Technology Models (PTMs) [1], achieves -106.553dBc/Hz at 1MHz offset, and dissipates 1.071mA from a 0.85V supply.**

***Index Terms* — FinFET, harmonic filtering, phase noise, power dissipation, tuned circuits, voltage-controlled oscillators.**

I. Introduction

In recent days, due to the immense growth of both wireless and optical communications systems, low-phase noise high frequency oscillator units have become a necessity. Local oscillators with as low as possible phase noise are useful to Radio Frequency (RF) transceivers' design, where the information signal is modulated or demodulated. During this process the bit-error-rate (BER) characteristic is highly dependent on the phase noise added by the VCO. Although Ring Oscillators (RO) are really simple and attractive topologies, from the standpoint of circuit integration, LC oscillators are the only means to achieve really good phase noise performance. The differential cross coupled LC oscillator with a source inductor and a capacitor in parallel with the current source, is well known for its good phase noise performance and ease of implementation [2]. This work evaluates these structures in 16nm FinFET CMOS using high performance Predictive Technology Model(s) and presents simulation results of such an oscillator operating at 16 GHz. According to simulation results, the circuit is capable of producing low-phase noise signals with a power consumption of almost 0.91mW that could be used in any CMOS transceiver of the previously mentioned frequency.

The rest of this paper is organized as follows. Section II presents the circuit design. Section III describes the phase noise improvement techniques and Section IV provides the results and a corresponding discussion. Section V summarizes this work.

II. Circuit Design

The schematic of the differential LC-oscillator is shown in Fig. 1. The main core of the oscillator consists of two cross-coupled nMos transistors and the LC-tank. Furthermore, we have implemented a simple current mirror, with a capacitor in parallel that provides the circuit with the current needed through a source inductor. The two cross-coupled transistors are responsible to provide the negative resistance amplifier stage, which in turn compensates for the resonator losses and at the same time stabilizes the oscillation.

The resonator, i.e. the LC-tank, consists of inductors and varactors which are also responsible for stabilizing the oscillation around our center frequency, f_o. Excluding the circuit's active elements, the passive elements constituting the resonator (inductors, varactors) are dominating the phase noise characteristics of our design and further degrade its performance.

To reduce the noise lossy inductors impose to our circuit, inductors with higher quality factors (Q) should be implemented leading to lower resistive loss and subsequently lower noise and power dissipation. However, the quality factor is limited by the integration technology and there is not much the designer could do towards this direction.

Inductors have been synthesized using VeloceRF™ inductor synthesis EDA tool which provides rapid modeling and synthesis of integrated inductors and transformers, with signoff accuracy for electromagnetic effects such as mutual

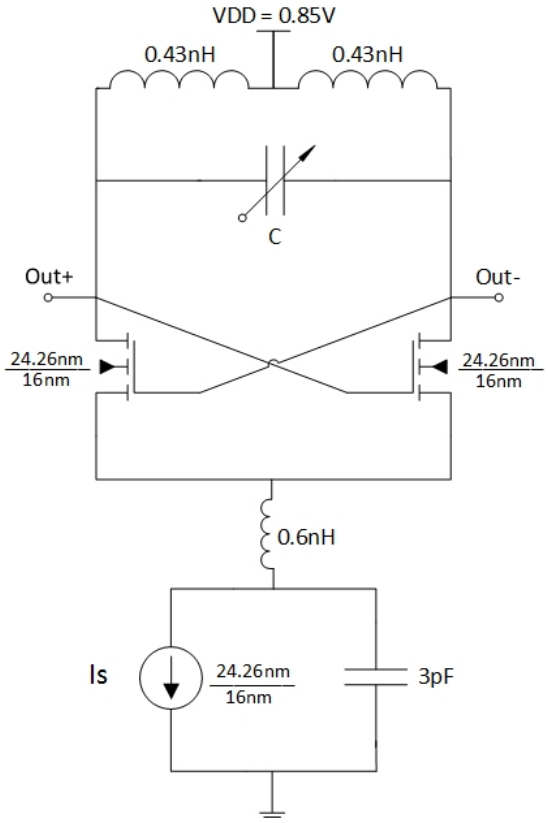

Fig. 1. VCO Schematic

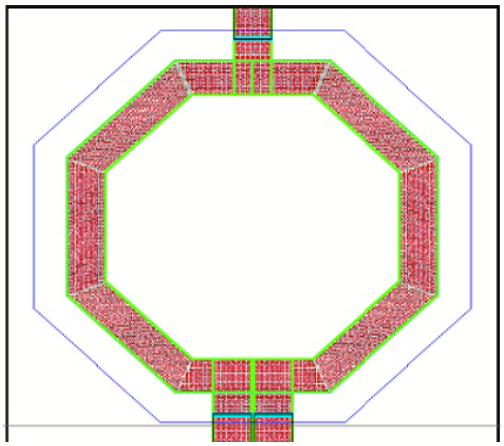

Fig. 2. Inductor Layout

inductance, skin effect and substrate losses. Details about the inductor are shown below. It consists of 2.6um thick Redistribution Layer (RDL) stacked with 3.2um thick copper stacked with 1.05um thick copper. *Q* is 29.38, *L* is 0.43 nH, Max*Q* freq is 16 GHz, Self Resonance Frequency (SRF) is higher than 48 GHz, area is 248 um x 248 um, track width is 10.38 um, and track distance is 2.01 um (Fig. 2).

In order to provide the desirable frequency fine-tuning in our design varactors are used. The overall phase noise performance of the LC-VCO presented is significantly affected by the design and modeling of the varactor. MOS-based Inversion type varactors were used due to their high *Q*-factor, wide tuning range, which improve with every new process generation, and implementation simplicity [3]. A pMOS-varactor has the same structure as a pMOS transistor, with its gate as the first terminal and drain-source as the second, while the bulk is connected directly to V_{DD}. In Fig. 3.A, we present the exact connection and the capacitance over the tuning range characteristic follows in Fig. 3.B.

Furthermore, several stages of the previously mentioned structure in parallel can be utilized in order to provide the specific capacitance needed (i.e. 0.15pF) for our center oscillation frequency.

Further, the C-V characteristics of a pMOS varactor could not be easily modeled, although we know the oscillation frequency is computed using the following equation:

$$f_o = \frac{1}{2\pi\sqrt{L \cdot C(V)}} \tag{1}$$

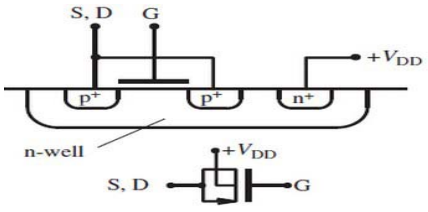

Fig. 3.A MOS Inversion Type Varactor Cross-section & Connection

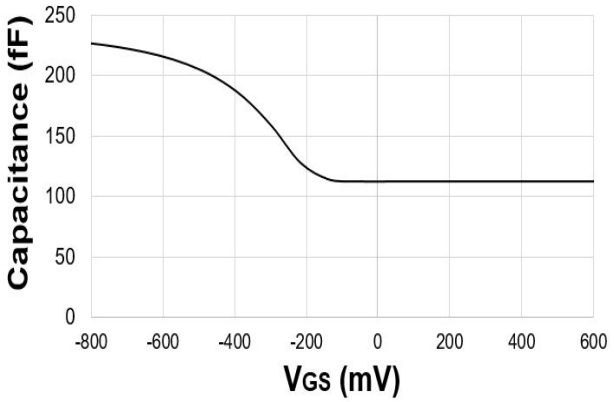

Fig. 3.B Capacitance – V_{GS} Curve

where *L* is the inductance and *C(V)* is the equivalent capacitance at a given biasing point.

Simply solving equation (1), we could get the norm to model *C(V)* given a certain oscillation frequency and inductance as follows:

$$C(V) = \frac{1}{4\pi^2 \cdot f_o^2 \cdot L} \tag{2}$$

Apart from all the preceding, it is critical to take into account that capacitance is dependent not only on the signal swing of the output but also on the contribution of the center frequency harmonics.

Additionally, the source inductor with the current mirror and the capacitor connected in parallel form a filtered current source, which improves significantly the phase-noise performance of the oscillator. Although, we would prefer the current source to be ideally noiseless and have a high impedance at $2f_o$(second harmonic frequency) to prevent the cross coupled pair from loading the resonator, this is not easily achieved.

A source inductor is therefore used to resonate the parasitic of the current source at $2f_o$ and the parallel capacitor reduces the high-frequency noise contribution of the current source providing path to ground [4]-[6]. Thus, to summarize this filtering technique prevents tail current noise at $2f_o$-using the source inductor- and reduces high-frequency noise-using the parallel capacitor. We have to also take into account the low-frequency tail current noise, which converts into phase-noise and is caused by the non-ideal behavior of the current source. To enable simulations the oscillator output drives a 350 load.

III. Phase Noise Improvement Techniques

Some of the most important phase noise contributors are the noise the tail current source feeds the circuit around the second harmonic frequency ($2f_o$), the noise due to the resistance of the cross-coupled transistors and the in-band noise of the *LC*-tank. The most difficult challenge in oscillator design is to simultaneously achieve low phase noise performance minimizing the contribution of the

previously mentioned factors and at the same time meet or even better exceed the oscillator specifications.

In this work, some of the most commonly used methodologies will be implemented and their effect on overall phase noise will be evaluated. The techniques that are mainly discussed are the resonator's quality factor, the increase in tail current and current source filtering.

1. *High Quality Factor(Q) Resonator*

In *LC* oscillator topologies the quality factor of the resonator is one of the most important design variables. We already know that the *Q*-factor of every *LC*-tank is constrained by the inductor's *Q*, given that inductors present a higher degree of energy dissipation as compared to capacitors. The dependence of phase noise to the resonator's quality factor can be attained from Leeson's formula as follows:

$$L(f_m) = 10\log\left[\frac{1}{2}\left(\left(\frac{f_o}{2 \cdot Q \cdot f_m}\right)^2 + 1\right)\left(\frac{f_c}{f_m} + 1\right)\left(\frac{FkT}{P}\right)\right] \quad (3)$$

where f_o is the output frequency, Q is the resonator Q, f_m is the offset from the carrier frequency(Hz), f_c is the *1/f* corner frequency, F is the noise factor of the amplifier, k is Boltzmann's constant, T is absolute temperature in Kelvin, and P is the oscillator output power.

Hence, a high *Q*-factor inductor would provide an *LC*-tank which would work as a very effective band-pass filter around the center frequency cutting off as many as possible noise components -ideally all. Furthermore, a high *Q*-factor indicates less *LC*-tank in-band noise and significantly bounds its losses, leading to much better phase noise performance and decreased power requirements to maintain oscillation. This method is the most efficient as compared to other techniques but is highly dependent on the integration technology dimensions, in our case 16nm. The simulated results presented in Table I prove that even a small improvement in the *Q*-factor can significantly affect phase noise. Our topology's enhancement reached over 2dBc with almost the same power consumption.

2. Increase Tail Current

Phase noise is the measure of purity of a local oscillator and its most critical specification. Since it is calculated as the ratio of noise power to output signal power in a 1Hz bandwidth at a given offset from the carrier signal,

TABLE I
Quality factor Contribution to Phase Noise

Q	Power(mW)	PN@1MHz(dBc/Hz)
5	0.425	-82.354
12	0.425	-96.325
25	0.425	-100.93

TABLE II
Tail Current Contribution to Phase Noise

I_{tail}(mA)	Freq(GHz)	PN@1MHz(dBc/Hz)
0.731	16.11	-99.871
0.960	15.99	-100.761
1.055	15.95	-101.126
1.530	16.08	-102.646
1.947	15.97	-104.22
2.849	16.15	-107.357

TABLE III
Current Source Filtering Contribution to Phase Noise

Source Filtering	Freq (GHz)	I_{tail} (mA)	PN@1MHz (dBc/Hz)
Without	15.89	1.071	-103.398
With	15.93	1.071	-106.553
Without	16.2	1.071	-102.941
With	16.03	1.071	-105.007

providing a larger signal to our circuit would improve phase noise. The easiest way to achieve a greater signal is by providing the circuit with higher tail current. However, better phase noise due to increased tail current comes at the expense of higher power dissipation, which is not always feasible. Furthermore, if the cross-coupled transistors have reached their saturation limit, no matter how much current is provided to the circuit, its output will remain unaffected. These are the main reasons this technique should be implemented with caution, bearing in mind that increased tail current induces further noise to the circuit, due to the non-ideal current source, and greater power consumption. In Table II, we have gathered some simulation results with regard to tail current and it is easily concluded that small increases in the current supplying our circuit can result to much better overall phase noise performance.

3. Current Source Filtering

A current source with almost ideal, noiseless, behavior is not easily achieved and all the non-linearities that stem from this phenomenon are converted in phase noise. In an effort to reduce these contributions a large capacitor is connected in parallel with the current source and shunts the high-frequency noise to the ground. In addition, to provide high impedance and at the same time resonate the parasitic of the current source at the second harmonic ($2f_o$) a source inductor is implemented connecting the current source with the cross-coupled transistors. The simulation results

provided in Table III show that for the exact same design and power consumption source filtering exhibits much better phase noise characteristics and should be therefore implemented wherever design constraints permit it.

IV. Results

The improvement current source filtering provided to our circuit is not negligible and can be observed in Fig. 4. Since the phase-noise performance at 1MHz offset from f_o is -106.553dBc/Hz for the source-filtered implementation while only -103.398dBc/Hz for the current source without inductive filtering.

Furthermore, the output frequency ranges from 14.31 to 17.06 GHz with control voltages varying from 0.2 to 0.8V. The center frequency of the implemented VCO, f_o, is 16GHz and the differential output is 3.259 dBm driving 350 loads at its output. It is also critical to observe the severe attenuation at the second harmonic due to $2f_o$ filtering, as presented in Fig. 5, which also improved phase noise.

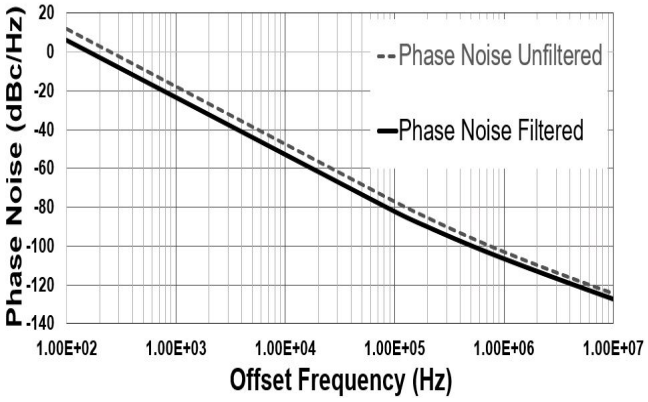

Fig. 4. Phase Noise performance, with and without Source Filtering

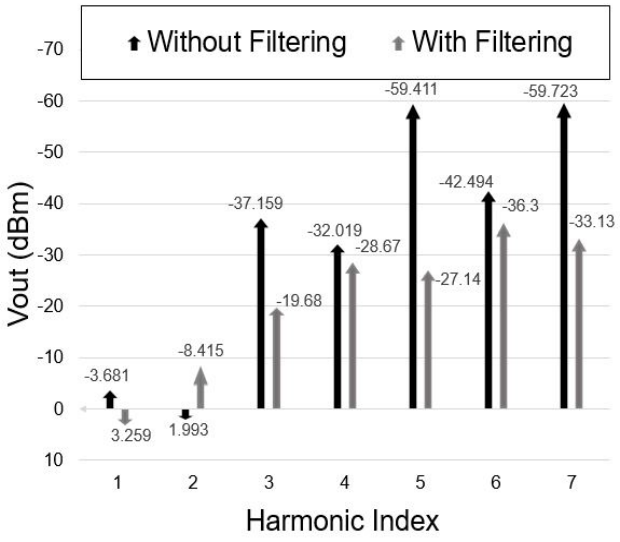

Fig. 5. Harmonic Amplitude in dBm, with and without Source Filtering

In order to evaluate different VCO designs apart from their Phase Noise, power dissipation and output power characteristics, which can be misleading at different implementations, other metrics are also used. Figure of Merit (FoM), can determine the efficiency of an oscillator taking into account both the Phase Noise at a specific offset frequency and the power consumption. The calculated FoM value provides the necessary abstraction to compare circuit topologies that might even have different oscillation frequencies and other process variations. In Table IV, other similar designs are presented and their performance parameters are outlined for comparison. FOM is calculated by Eq. (4):

$$FOM = 10log_{10}\left(\left(\frac{f_o}{\Delta f}\right)^2 * \left(\frac{1}{P * 10^{\frac{L(\Delta f)}{10}}}\right)\right) \quad (4)$$

where f_o is the oscillation frequency, f is the offset frequency from the carrier (1MHz in our case), P is the power consumption in mW and $L(f)$ is the Phase Noise at the mentioned offset frequency

Due to the immense growth of wireless technology, oscillators with wide tuning range are demanded. However, the conventional FoM does not consider the frequency tuning range, which degrades the phase noise drastically.

In Table V, a variation of the traditional FoM is used which takes into account the tuning range provided by the design for benchmarking purposes. The proposed work compares favorably against similar VCOs, exhibiting decent results for FoM and the tuning aware FoM formula mentioned below:

$$FOM_T = 10log_{10}\left(\left(\frac{f_o * tuning\%}{10\Delta f}\right)^2 * \left(\frac{1}{P * 10^{\frac{L(\Delta f)}{10}}}\right)\right) \quad (5)$$

where f_o is the oscillation frequency, *tuning%* is the tuning percentage (in our case 2.75GHz/16GHz = 17.2%), f is the offset frequency from the carrier (1MHz in our case), P is the power consumption in mW and $L(f)$ is the Phase Noise at the mentioned offset frequency

V. Conclusions

In this work, a 16GHz differential LC VCO using an inversion-type varactor has been implemented in 16nm FinFET technology. The simulated tuning range of the oscillator is 17.2%. A number of phase noise reduction techniques have been evaluated. Good phase noise performance is achieved over the entire tuning range, reaching -106.553dBc/Hz at 1 MHz offset from f_o. The power consumption of the proposed core design is 0.91mW, since 1.071mA is drawn from a 0.85V supply

TABLE IV
VCO Figure of Merit Performance

Ref	Process	Freq GHz	PN@1MHz dBc/Hz	Power mW	FoM dB
This Work	FinFET 16nm (PTM)	16	-106.553	0.91	191
[7]	FinFET 80nm	15.3	-94	7.5	169
[8]	32nm SOI CMOS	23.5	-96	13.5	172
[9]	28nm FDSOI CMOS	42.2	-98	6	183

TABLE V
VCO Tuning Range aware FOM Performance

Ref	Process	Freq GHz	PN@1MHz dBc/Hz	Tuning Range %	FoM_T dB
This Work	FinFET 16nm (PTM)	16	-106.553	17.2	195.8
[7]	FinFET 80nm	15.3	-94	5	162.9
[8]	32nm SOI CMOS	23.5	-96	30	181.6
[9]	28nm FDSOI CMOS	42.2	-98	18.5	188

under typical conditions. All the preceding, lead to a Phase Noise Figure of Merit (*FoM*) of 191dB, which when tuning range is also accounted for (FoM_T), reaches 195.8dB.

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