

A 5 GHz LOW NOISE AMPLIFIER ON 0.35 μm BiCMOS SiGe

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ABSTRACT

The Low Noise Amplifier (LNA) presented in this work offers a gain of 20 dB, a noise figure of 1.6 dB, with an input referred third-order intercept point of -4.5 dBm and a 1 dB compression point of -16 dBm at 5.2 GHz, using 0.35 μm BiCMOS SiGe. It operates on 5 V and requires 10 mA. The output and the input of the amplifier are matched internally to 50 Ω. The amplifier includes an image reject filter, an adaptive bias network, an RLC tank and input / output balun transformers. The image reject filter attenuates the image signal by providing low impedance at that frequency and is tuned by voltage control. An adaptive bias network is used, which allows the user to select the bias current in an adaptive manner, depending upon the requirements of the individual system. (Low NF, high gain, low consumption etc.)

1. INTRODUCTION

The 5 GHz wireless LAN market grows rapidly and offers various benefits to the user. 5 GHz LAN technology supports multimedia services, real time voice and video transfer, and other bandwidth intensive applications. However, the design, integration and fabrication of high quality components at 5 GHz frequencies are very demanding. One of the most critical parts of the front-end is the low noise amplifier, which sets the noise figure of the receiver and enhances the signal before demodulation.

Low noise amplifier design is required to meet several goals, such as minimizing the noise figure and the power consumption, providing high gain, linearity and input / output matching. At high frequencies, where the Miller effect is increased, cascode configurations are frequently preferred. In recent years low noise amplifiers with good performance have been reported especially in CMOS technology [1-4]. In this paper we present the design of a bipolar amplifier with a tunable image reject filter, which uses MOS transistors.

Referring to the single-ended cascode amplifier (Fig. 1) we note that the common-emitter device determines the overall noise figure, which is given by [5]:

$$NF = 1 + \frac{r_b + r_e}{R_s} + \frac{g_m \cdot R_s}{2 \cdot \beta} + \frac{1}{2 \cdot \beta \cdot g_m \cdot R_s} \cdot \left(\frac{\omega_T}{\omega_0} \right)^2 + \frac{g_m \cdot R_s}{2} \cdot \left(\frac{\omega_0}{\omega_T} \right)^2 + \frac{4 \cdot R_s}{R_C} \cdot \left(\frac{\omega_0}{\omega_T} \right)^2 \quad (1)$$

The conditions to achieve matching employing inductive degeneration are [5]:

$$\omega_T \cdot L_E + r_x + r_\pi \cdot \left(\frac{\omega_T}{\omega_0 \cdot \beta} \right)^2 \cong R_s \quad (2a)$$

$$\omega_0^2 \cdot (L_B + L_E) \cdot (C_\pi + C_\mu) \cong 1 \quad (2b)$$

Equation 2a shows that at resonance, which is determined by input inductance L_B , the input impedance is almost real and proportional to L_E .

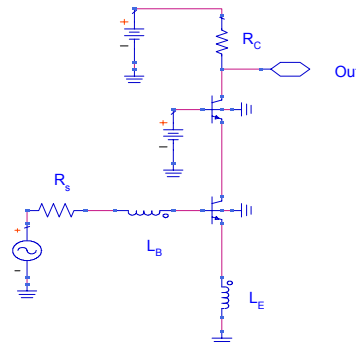


Figure 1. Cascode topology with matching elements.

In section 2 we present the differential cascode topology, in section 3 the design of the tunable image reject filter and in sections 4 and 5 the input / output balun transformers and the adaptive bias network respectively. The simulation results in this work were obtained using ADS 2002[®].

2. DIFFERENTIAL CASCODE TOPOLOGY

Differential cascode topology offers important advantages in terms of noise, bandwidth and reverse isolation. In addition to these, the parasitic source degeneration is obliterated and the interference produced inside the chip after the implementation is significantly

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lower with respect to the single-ended structures. Input and output transformers are used to do the conversion from single-ended to differential and vice versa.

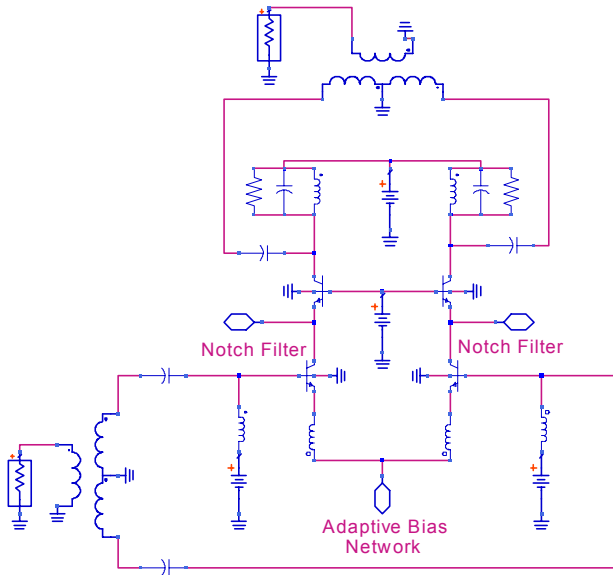


Figure 2. Differential cascode topology, including matching elements and input / output transformers.

As we have mentioned before, the common emitter device determines the overall noise figure of the amplifier. For such a device there is an optimum source impedance (not necessarily 50 Ω) given by [6]:

$$R_{s-opt} = \left(\frac{1}{M \cdot N} \right) \left[\frac{f_T}{f} \left(\frac{n^2 \cdot V_T}{2 \cdot J_c} + (r_e + r_b)_u \right) \right] \cdot \left[\frac{\sqrt{\frac{J_c}{2 \cdot V_T} (r_e + r_b)_u \cdot \left(1 + \frac{f_T^2}{\beta_{DC} \cdot f^2} \right) + \frac{n^2 \cdot f_T^2}{4 \cdot \beta_{DC} \cdot f^2}}}{\frac{J_c}{2 \cdot V_T} (r_e + r_b)_u \cdot \left(1 + \frac{f_T^2}{\beta_{DC} \cdot f^2} \right) + \frac{n^2}{4} \cdot \left(1 + \frac{f_T^2}{\beta_{DC} \cdot f^2} \right)} \right] \quad (3)$$

where the subscript u corresponds to the base-emitter resistance sum of a single (unit) device, J_c is the collector dc current density, f_T is the unity current gain frequency, n is the junction grading factor (taking values from 1 to 1.2), V_T is the threshold voltage and $M \cdot N$ is the device size relative to the unit device. There is an optimum $M \cdot N$ product for which R_{s-opt} could be equal to 50 Ω . The minimum NF is then given by [6]:

$$NF_{min}(J_c) = 1 + \frac{n}{\beta_{DC}} + \sqrt{\frac{J_c}{2 \cdot V_T} (r_e + r_b)_u \cdot \left(1 + \frac{f_T^2}{\beta_{DC} \cdot f^2} \right) + \frac{n^2}{\beta_{DC}}} \quad (4)$$

To achieve the minimum noise figure the designer should select the appropriate current density. In Figure 3 we

show the simulation results of the minimum noise figure versus the current density.

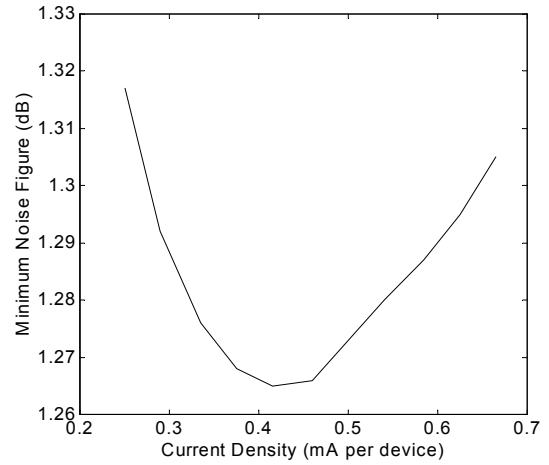


Figure 3. Minimum NF versus current density.

As the optimum bias current, we selected the value of 0.41 mA per device. It will be shown in the next section that the amplifier is able to operate with different bias currents while exhibiting very good performance. The tuned amplifier provides selective amplification and considerably lower power consumption. In combination with the notch filter, it rejects the unwanted signals. The tank is a parallel RLC network.

3. THE TUNABLE IMAGE REJECT FILTER

Image frequency is an undesired signal twice the IF frequency above or below the useful radio frequency depending on whether upper or lower LO injection is used. An image reject filter is always needed before the mixer to attenuate this signal [7].

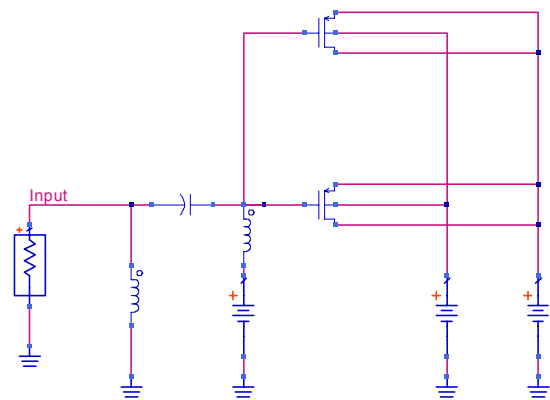


Figure 4. The notch filter using the I-mode MOS varactor.

The gain curve of the low noise amplifier including the image reject (notch) filter is shown in Figure 5. The filter includes an inductor, a capacitor and an I-mode MOS varactor. Two identical filters are connected to the collectors of both the common-emitter devices of the differential amplifier. A 9 dB attenuation is achieved at

the image frequency in contrast to more than 20 dB gain at the center frequency.

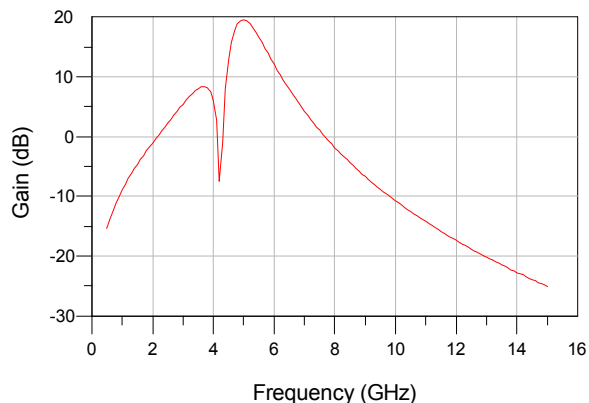


Figure 5. The result of the Notch filter at the gain of the LNA.

The image reject filter (notch filter) is tuned by an inversion-mode MOS varactor which is controlled by an external voltage. The two p-MOS transistors shown in Figure 4 implement the I-mode MOS varactor.

This technique provides the advantage of rapid capacitance variations for small tuning voltage variations. (0.4 pF for 100 mV voltage variation). The notch of the filter is swept from 4.5 GHz - 4.9 GHz for 2.6 V to 2.4 V tuning voltage respectively. The slope of the tuning voltage versus frequency curve at 4.7 GHz, which is the center frequency of the image filter, is 2 MHz/mV.

4. THE INPUT / OUTPUT BALUN TRANSFORMERS

The transformer improves the input matching and the maximum available output gain but introduces further noise. Furthermore we could not achieve the minimum noise figure, shown in Figure 6. On this plot the minimum noise figure and the succeeded noise figure is plotted for 1:1 ratio of transformer turns. The transformer is used only to convert the single-ended signals to differential and vice versa in that case. It is obvious that within the frequency range of operation the actual noise figure is very close to the minimum noise figure.

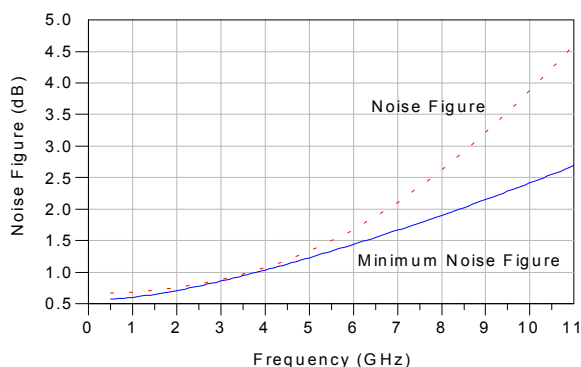


Figure 6. The noise figure and the minimum noise figure of the LNA.

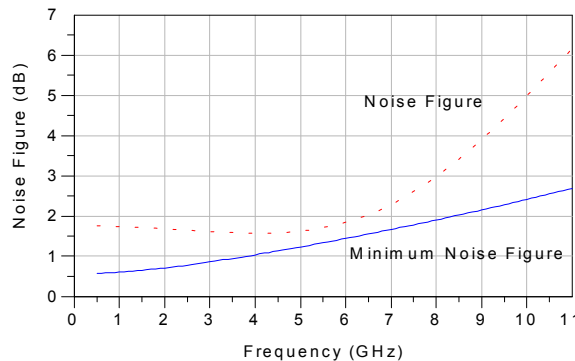


Figure 7. The noise figure and the minimum noise figure of the LNA for the selected ratio of turns.

To produce best input matching and maximum available gain we had to change the ratio of turns. Through simulation it was found that for $n = 1:2$ the achieved NF (Fig. 7) departs from the one before. Comparing Figures 6 and 7 we can verify that the transformers introduce extra noise and prevent us from achieving the minimum noise figure.

5. THE ADAPTIVE BIAS NETWORK

An adaptive bias network has been used to select the desirable bias current depending on the required objective: maximum performance, low consumption, or a combination of both the above options. The selection of the desirable bias current is achieved by a 5-bit signal. The configuration of this circuit is as shown in Figure 8. If one of the five bits is high and the other four are low, the corresponding transistor is active and the selected current runs through the corresponding resistance. The topology is completed with an improved current mirror using an extra transistor. This transistor reduces the part of the reference current used to drive the two identical transistors of the simple current mirror.

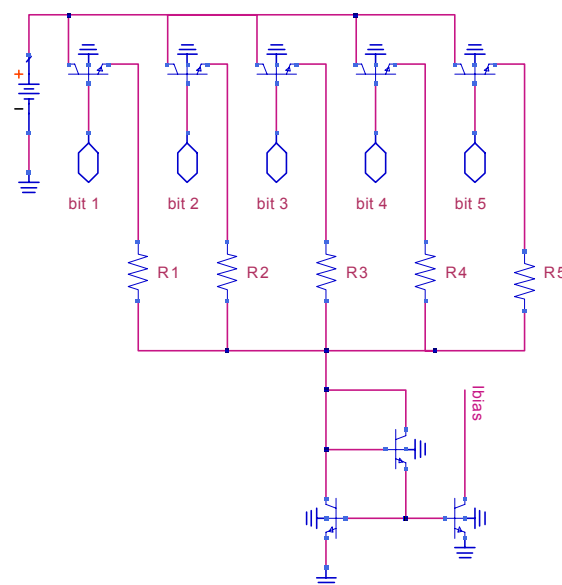


Figure 8. The adaptive bias network.

Using this adaptive bias network the amplifier is able to operate consuming five different values of I_c . The noise figure, the gain and the input impedance for each one is presented in the results section. By careful design of the input matching, the noise figure is kept at low levels for all the different bias currents whereas the gain does not change significantly.

6. RESULTS

Table 1 summarizes the simulated results such as the noise figure, available gain and input impedance for the different values of I_c .

Table 1. Noise figure, gain, input impedance for the 5 different possible bias currents

I_c	NF	Gain	Re[Z(1,1)]	Im[Z(1,1)]
4	1,8	15	41	-18
6	1,7	17	46	-9,0
8	1,6	18	51	-2,4
10	1,6	19	55	2,7
12	1,6	19	58	7,0

The shape of the gain curve, is as shown in Figure 9 for bias currents from 4 mA to 12 mA. From the simulation results we noticed that within a considerable bandwidth (more that 500 MHz) the gain variation is very small (0.5 dB)

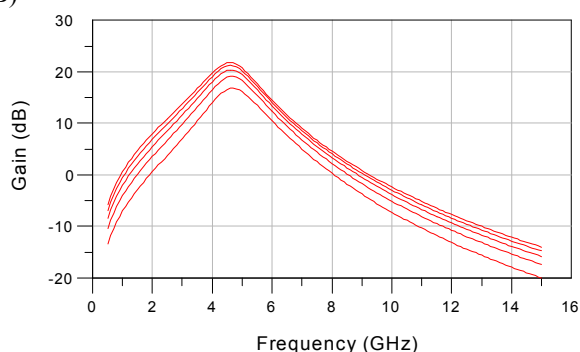


Figure 9. The Gain of the LNA.

The NF for the same bias currents is also plotted in Figure 10.

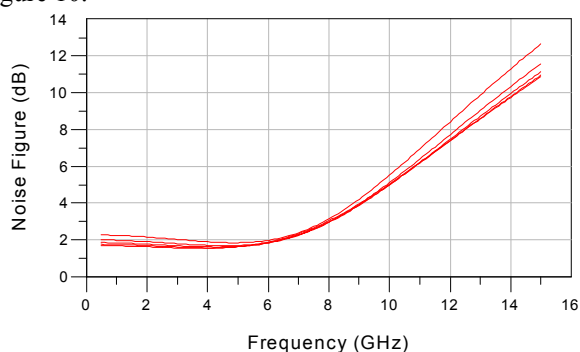


Figure 10. The Noise Figure of the LNA.

In Table 2, the input P_{1dB} and input IP3 for different values of I_c are presented.

Table 2. Input P_{1dB} , input IP3 at 5.2 GHz for the 5 different possible bias currents

I_c (mA)	Input P_{1dB} (dBm)	Input IP3 (dBm)
4	-20	-14
6	-18	-10
8	-17	-7
10	-16	-4.5
12	-14	-2.4

7. CONCLUSIONS

A 5.2 GHz variable gain low noise amplifier has been demonstrated using a differential cascode topology. The amplifier comprises of a tunable image reject filter an adaptive bias network, which allows for different collector currents and a resonant RLC tank. Simulated results produced a NF of 1.6 dB, a gain of 20 dB, a P_{1dB} of -16 dBm and an IP3 of -4.5 dBm at 5.2 GHz. The tuning range of the notch filter is from 4500 GHz to 4900 GHz and the image rejection at 4.7 GHz is 10 dB. An I-mode MOS varactor, controlled by an external voltage, is used to tune the filter. Input and output transformers are used to generate differential inputs and combine differential outputs to single-ended. Currently, the chip layout is designed for fabrication in a 0.35 μ m BiCMOS SiGe process.

8. REFERENCES

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