A 5-GHz, Variable Gain, SiGe Low Noise Amplifier

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Abstract - A bipolar low noise amplifier (LNA) is described in this work. The IC contains the LNA core, an externally programmed bias network, a voltage divider, an LC tank and inductors to set the input impedance. The externally programmed bias network allows the user to select the bias current in an adaptive manner, depending upon the requirements of the individual system. (Low NF, high gain, low consumption etc). The chip can be powered down by sending an appropriate bit stream to the bias network. The tuned amplifier using a parallel LC network provides selective amplification and lower power consumption. The produced gain is 15 dB while the NF is 2.1 dB for moderate power consumption. The IIP3 is –7 dB and the P_{1dB} is –17 dB. The power consumption from a single 5-V supply is 3.4 mA for the low gain mode and 13 mA for the high gain mode.

I. INTRODUCTION

Wireless local area networks operating in 5 GHz band are very popular because of their high transfer rates and low implementation cost. The 5 GHz market becomes more and more established, grows rapidly and offers various benefits to the user. WLAN systems support multimedia services, real time voice and video transfer, and other high data throughput applications. However, the design and implementation of a high quality RF front - end should meet demanding performance requirements. One of the most critical parts of a receiver front - end is the low noise amplifier. Low noise figure and sufficient gain are required. In addition, input and output impedance matching, linearity and power consumption are some goals, which should be met.

Although significant work has been done in CMOS process for low noise amplifiers [1-4] the development of SiGe bipolar amplifier is very challenging and promising. In this paper we build a bipolar low noise amplifier while MOS transistors are only used for the biasing networks.

The SiGe BiCMOS process used for this design includes 35-GHz f_T NPN's 0.35-μm L_{eff} CMOS plus four layers of metal. In section II we present the optimum topology, section III describes the design of the bias networks and finally the results are presented in section IV.

II. OPTIMUM ARCHITECTURE

At high frequencies, where the Miller effect is increased, the cascode topology with inductive degeneration is frequently preferred [5]. Furthermore, is a

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simple structure, which offers low noise, high gain and stability. Referring to the single-ended cascode LNA we note that the common-emitter device determines the overall noise figure, which is given by [6]:

$$NF = 1 + \frac{r_b + r_e}{R_s} + \frac{g_m \cdot R_s}{2 \cdot \beta} + \frac{1}{2 \cdot \beta \cdot g_m \cdot R_s} \cdot \left(\frac{\omega_T}{\omega_0}\right)^2$$
$$+ \frac{g_m \cdot R_s}{2} \cdot \left(\frac{\omega_0}{\omega_T}\right)^2 + \frac{4 \cdot R_s}{R_C} \cdot \left(\frac{\omega_0}{\omega_T}\right)^2 \quad (1)$$

The conditions to achieve matching employing inductive degeneration are [6]:

$$\omega_T \cdot L_E + r_x + r_\pi \cdot \left(\frac{\omega_T}{\omega_0 \cdot \beta}\right)^2 \cong R_s \quad (2a)$$

$$\omega_0^2 \cdot (L_B + L_E) \cdot (C_\pi + C_\mu) \cong 1 \quad (2b)$$

Equation 2a shows that at resonance, which is determined by input inductance L_B, the input impedance is purely real and equal to $\omega_T \cdot L_E$.

As we have mentioned before, the common emitter device determines the overall noise figure of the amplifier. For such a device there is an optimum source impedance (not necessarily 50 Ω) given by [7]:

$$R_{s-opt} = \left(\frac{1}{M \cdot N}\right)\left[\frac{f_T}{f}\left(\frac{n^2 \cdot V_T}{2 \cdot J_c} + (r_e + r_b)_u\right)\right] \cdot$$
$$\cdot \left[\frac{\sqrt{\frac{J_c}{2 \cdot V_T}(r_e + r_b)_u \cdot \left(1 + \frac{f_T^2}{\beta_{DC} \cdot f^2}\right) + \frac{n^2 \cdot f_T^2}{4 \cdot \beta_{DC} \cdot f^2}}}{\frac{J_c}{2 \cdot V_T}(r_e + r_b)_u \cdot \left(1 + \frac{f_T^2}{\beta_{DC} \cdot f^2}\right) + \frac{n^2}{4}\cdot\left(1 + \frac{f_T^2}{\beta_{DC} \cdot f^2}\right)}\right] \quad (3)$$

where the subscript u corresponds to the base-emitter resistance sum of a single (unit) device, J_c is the collector dc current density, f_T is the unity current gain frequency, n is the junction grading factor (taking values from 1 to 1.2), V_T is the threshold voltage and $M \cdot N$ is the device size relative to the unit device. There is an optimum $M \cdot N$ product for which R_{s-opt} could be equal to 50 Ω. The minimum NF is then given by [7]:

$$NF_{min}(J_c) = 1 + \frac{n}{\beta_{DC}} +$$
$$+ \sqrt{\frac{J_c}{2 \cdot V_T}(r_e + r_b)_u \cdot \left(1 + \frac{f_T^2}{\beta_{DC} \cdot f^2}\right) + \frac{n^2}{\beta_{DC}}} \quad (4)$$

To achieve the minimum noise figure the designer should select the appropriate current density. In Fig. 1 we show

the simulation results of the minimum noise figure versus the current density for the specific process we used.

Fig. 1. Minimum NF versus current density.

The simple cascode structure can be extended to the cascode differential configuration, which offers important advantages in terms of noise, bandwidth and reverse isolation [8]. In addition to these, the parasitic source degeneration is obliterated and the interference produced inside the chip after the implementation is significantly lower with respect to the single-ended structures. The differential inputs and outputs of the LNA must be coupled to the single ended output and input of the previous and following stages. An off-chip balun is used to achieve this conversion.

Fig. 2. The differential-cascode topology, including matching elements.

The core of the low noise amplifier is shown in Fig. 2. The large differential transistors are split into smaller, parallel transistors, for better noise performance. The amplifier is able to operate with different bias currents while exhibiting very good performance. The tuned amplifier provides selective amplification and considerably lower power consumption. The tank is a parallel LC network.

III. THE BIAS NETWORKS

An externally programmed bias network using PMOS transistors has been used. The objective of this network is to deliver DC power to the device, providing seven modes of operation (seven different bias currents) and a sleep mode. The desirable bias current can be selected depending on the required objective: high gain and low NF, low consumption, or a combination of both the above options. The selection of the desirable bias current is achieved by a 3-bit signal. The configuration of this circuit is as shown in Fig. 3. If one of the three bits is low and the other two are high, the corresponding transistor is active and the selected current runs through the corresponding resistance. In addition to this there are 2^3 total modes. The topology is completed with an improved current mirror using an extra transistor. This transistor reduces the part of the reference current used to drive the two identical transistors of the simple current mirror.

Fig. 3. The externally programmed bias network.

Using this externally programmed bias network the amplifier is able to operate consuming seven different values of I_c. The noise figure, the gain and the input impedance for each one are presented in Table I in the results section. Different modes of operation associated with 7 different bias currents and a sleep mode are available. By careful design of the bias network the noise figure is kept at low levels for all the different bias currents whereas the gain does not change significantly except for the lowest I_c. As the optimum bias current, we selected the value of 0.15 mA per device. This current provides the minimum noise figure and relatively low power consumption. Increasing or decreasing the current density by small value, the noise figure increases a little while the gain and the power consumption increase also. The noise figure variation is small enough, so, a higher gain mode can

be selected if the increment of the noise figure and the power consumption is not critical. It will be shown in the next section that the amplifier is able to operate with different bias currents while exhibiting very good performance even if the use of the external balun transformers decrease the gain and increase the noise figure.

To bias the base-emitter junctions of the differential transistors a voltage divider using MOSFET transistors (Fig. 4) has been used, were $\frac{W_{M1}}{W_{M2}} = 10$.
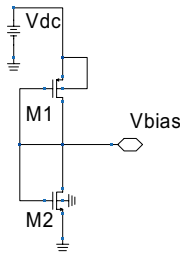

Fig. 4. The voltage divider.

IV. LAYOUT AND RESULTS

The layout of the LNA is shown in Fig. 5 and the layout of the adaptive network is shown in Fig. 6. The total layout figure is split into several parts for better viewing. Symmetrical splitting transistors and dummy resistors are used. The common-centroid technique is adopted in the biasing stage.
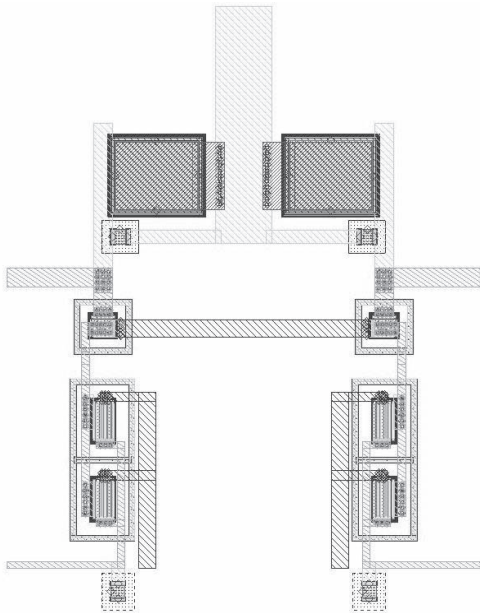
Fig. 5. The layout of the LNA core.
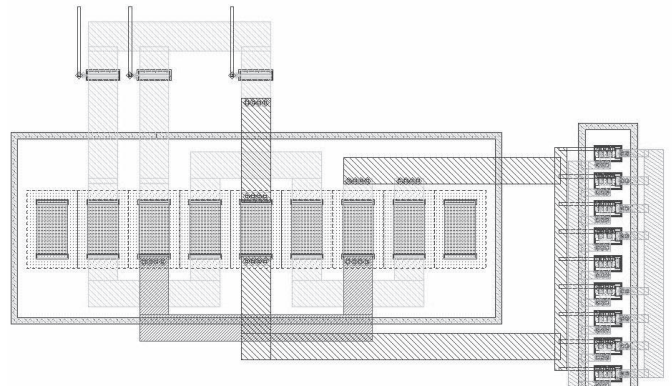
Fig. 6. The layout of the externally programmed bias network.

On-chip spiral inductor L_E is used to set the real part of the input impedance equal to 50 Ω, while on-chip spiral inductor L_B sets the imaginary part of the input impedance equal to zero. The Q of the inductors is estimated to be about seven.

The on-chip spiral inductor L_B (1.1 nH) which is also used in the LC tank, is shown in Fig. 7.
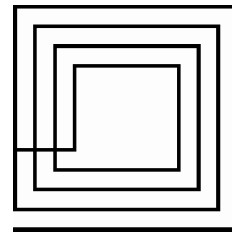

Fig. 7. The inductor L_B.

The shape of the gain curve is as shown in Fig. 9 for bias currents from 3.4 mA to 13 mA. From the simulation results we noticed that within a considerable bandwidth (more that 500 MHz) the gain variation is very small (0.5 dB)
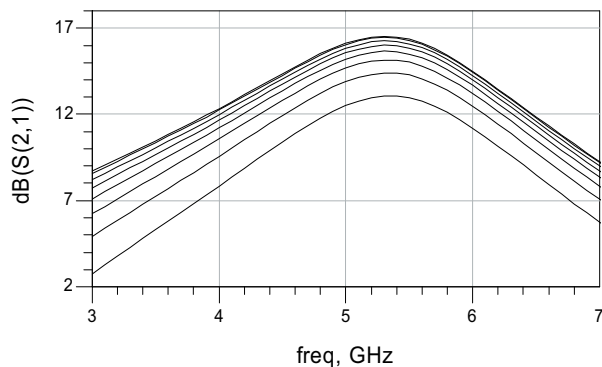

Fig. 9. The gain of the Low Noise Amplifier.

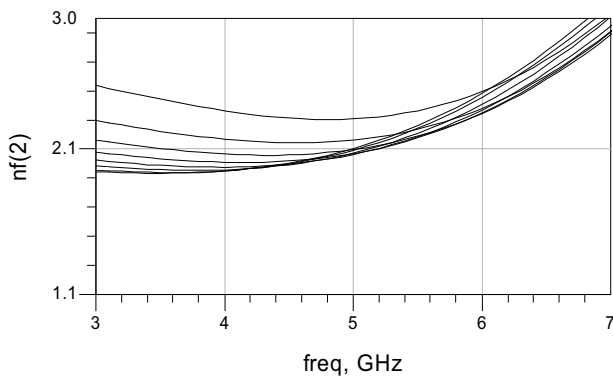The NF for the same bias currents is also plotted in Fig. 10.

Fig. 10. The NF of the Low Noise Amplifier.

Table I summarizes the simulated results such as the noise figure, available gain and P_{1dB} for the different values of I_c.

TABLE I
NOISE FIGURE , GAIN AND P_{1dB} FOR THE 7 POSSIBLE BIAS CURRENTS

3-bit control	I_C	NF	Gain	P_{1dB}
111	Sleep mode	Sleep mode	Sleep mode	Sleep mode
110	3.4	3.3	13.0	-20
101	5.8	2.2	14.3	-18
100	8.0	2.1	15.0	-17
011	9.0	2.1	15.5	-16
010	10	2.1	16.0	-14
001	12	2.2	16.2	-12
000	13	2.3	16.5	-10

In Table II, the input impedance and the input IP3 for different values of I_c are presented.

V. CONCLUSIONS

We have demonstrated a 5.2 GHz variable gain low noise amplifier using a cascode differential architecture and on-chip inductors. The amplifier includes an externally programmed bias network and a resonant LC tank. The bias network is designed to provide seven different bias modes; subsequently the amplifier delivers different gain modes and a sleep mode. Simulated results produced a NF of 2.1 dB, a gain of 15 dB, a P_{1dB} of -17 dBm and an IIP3 of -7 dBm at 5.2 GHz. The power consumption for the mode of operation, which provides the above performance, is 8 mA from a single 5-V supply. External input and output transformers are used to generate differential inputs and combine differential outputs to single-ended. This also facilitates measurements for characterization of the chip which has currently been sent for fabrication.

TABLE II
Z_{IN} AND IIP3 FOR THE 7 POSSIBLE BIAS CURRENTS

3-bit control	I_C	RE[Z(1,1)]	Im[Z(1,1)]	IIP3
111	Sleep mode	Sleep mode	Sleep mode	Sleep mode
110	3.4	2.5	10.7	-14
101	5.8	2.2	16	-10
100	8.0	2.1	17	-7
011	9.0	2.1	17.7	-4.5
010	10	2	18.5	-2.4
001	12	2	19	0
000	13	2	19.7	2.0

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