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Design and Implementation of a Dual-Loop Frequency Synthesizer for 5 GHz WLANs

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Abstract **- This paper describes the design and implementation of a dual phase locked loop synthesizer that can match the specifications for wireless LANs operating at 5 GHz. It generates signals in the 4850 MHz to 5050 MHz range with a 10 MHz resolution. To have a flexible design discrete elements are used for implementing the upper and lower frequency loops. This flexibility in implementation gives the capability to experimentally optimize the trade-offs in order to achieve low phase noise and low spurious levels. This resulted in a prototype with very good characteristics suitable for future integration.**

I. INTRODUCTION

While the dual – loop implementation of a frequency synthesizer has been long replaced by the fractional - N integrated PLL architecture, it can still offer many benefits when stringent frequency accuracy specifications and phase noise requirements for radio frequency (RF) synthesizers are needed. A simple integer – N PLL architecture is not adequate to generate a high local oscillator (LO) frequency at 5 GHz because it must satisfy both resolution and phase noise requirements. This is due to the narrow bandwidth of the loop and the high value that the division ratio N of the loop divider must have, in order to maintain a low reference frequency for fine resolution [1, 3]. The dual – loop PLL architecture employs two loops to improve the trade – off between these two factors that determine the performance of a frequency synthesizer.

We propose a system where the divider is placed before the mixer. In contrast to previous dual-loop architectures this provides significant implementation advantages because the mixer needed is designed in a significantly lower frequency range.

Section II discusses the design of the synthesizer and the advantages of a dual – loop architecture. The implementation of the frequency synthesizer and the experimental results are presented in section III.

II. DUAL – LOOP SYNTHESIZER DESIGN

While the integer – N PLL architecture is the most popular, simple and inexpensive way to implement a frequency synthesizer, it fails to meet simultaneously the locking speed, channel spacing, reference frequency and phase noise requirements when frequencies as high as 5 GHz are to be generated. In integer – N frequency synthesizers, the channel spacing is equal to the reference frequency of the loop. Another drawback is that the output frequency changes by only integer multiples of the reference frequency. Compared to that, in the dual loop architecture, lower frequency division ratios are found with larger reference frequencies.

In fractional-N synthesizers the output frequency fluctuates by a fraction of the reference frequency. Increased loop bandwidth and consequently better locking speed and lower close-to-the-carrier phase noise due to the VCO is achieved. The main disadvantage of this architecture is the large fractional sidebands at the output.

Fractional-N with sigma-delta modulation technique reduces spurious level and fractional sidebands however this is a very complicated topology to design and implement.

Dual loop architecture presents comparable performance to fractional–N with delta-sigma modulation architecture [1]. Both can achieve satisfactory phase noise specifications, locking speed and spurious level and require similar chip area. The main advantage of the dual-loop technique is the simple prescaler with reduced division ratios and the restricted usage of digital circuitry. However two reference sources are required.

In order to achieve finer resolution at the high frequency output of the synthesizer, a low reference frequency is required, thus limiting its bandwidth and locking speed and resulting in large frequency division ratios. Furthermore, the design of the N programmable counter can become very complicated and inefficient [3].

The relationship between the channel spacing and reference frequency can be altered by employing two loops to implement the synthesizer, thus improving the trade – off between resolution and phase noise [1, 4].

A first simple approach of the dual – loop architecture is the parallel architecture a block diagram of which is shown in Fig. 1. The upper loop generates a fixed high – frequency signal, while the lower loop produces the variable, low – frequency steps that define the resolution of the synthesizer [2]. A single side band mixer (SSB) is employed to add the generated frequencies.

In the proposed architecture the two loops are combined in series. This is in contrast to the parallel architecture, where the SSB mixer is placed at the output of the two loops. In the series architecture the mixer is placed within one of the loops. The SSB mixer is a highly nonlinear device, which exhibits large spurs at its output. Therefore, placing it within one loop helps improve the quality of the signal at the output of the synthesizer due to the sideband suppression properties of PLLs [2]. As shown in Fig. 2, the SSB mixer is a part of the high frequency loop. In this way the sidebands are suppressed by both the low – pass filter at the output of the mixer and the M divider of the loop.

The price to be paid for the good quality signal achieved through this architecture is the longer settling time of the synthesizer. Although the parallel architecture ensures faster settling time, the series architecture is preferably used in wireless applications where noise and sidebands can severely damage information signals [4].

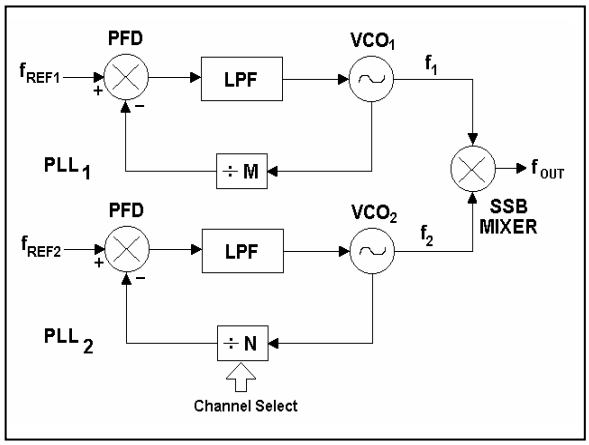

Fig. 1: Dual – loop parallel architecture.

The frequency synthesizer for our application must generate signals in the frequency range of 4850 MHz to 5050 MHz, with 10 MHz channel spacing. A typical phase noise value of – 100 dBc/Hz at 1 MHz away from carrier and approximately – 120 dBc/Hz at 10 MHz, are required to accommodate for modulations of high spectral efficiency (16-QAM, 64-QAM) which are used in modern WLANs.

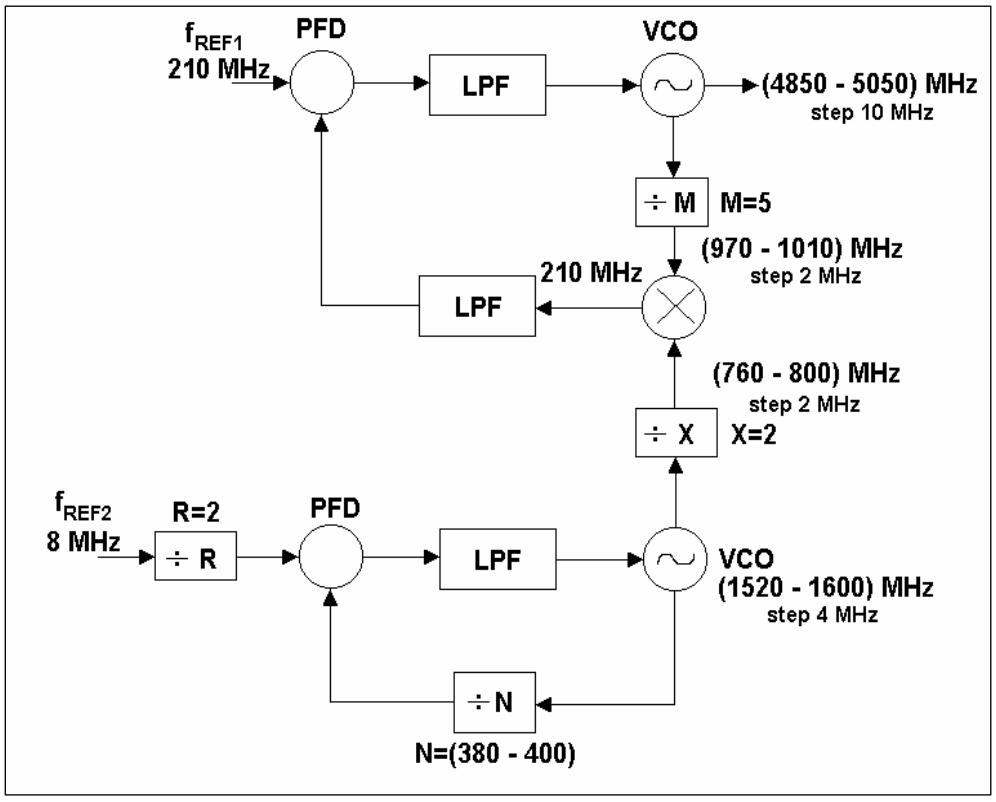

Fig. 2: Block diagram of the implemented dual – loop frequency synthesizer.

The block diagram of the proposed dual – loop architecture is shown in Fig. 2. The upper loop generates a fixed high – frequency signal, while the lower loop provides the variable low – frequency signal that determines the resolution of the synthesizer. A single sideband mixer is employed to subtract the divided – by – X (prescaler) low frequency loop output signal from the divided – by – M output signal of the synthesizer.

The main advantage of the dual – loop architecture is that it enables us to maintain a large bandwidth of the high – frequency loop by keeping its reference frequency high [1]. Thus, the phase noise of the output signal and the settling time are improved, while the resolution of the synthesizer remains unaffected, as it is determined by the reference frequency of the low – frequency loop.

Furthermore, a larger reference frequency allows for much lower frequency division ratios, which also helps improve the output signal phase noise [3]. The X prescaler helps increase the resolution of the lower – frequency loop without reducing the reference frequency of the lower loop. It also helps suppress the phase noise present at the output of the lower – loop voltage control oscillator (VCO) before it is fed into the SSB mixer [1].

Compared to other dual – loop architectures reported [1, 7], in the proposed one, the high frequency divider M is placed within the high frequency loop but before the SSB mixer. The divider provides satisfying reduction of the phase noise and attenuates the sidebands produced by the VCO, before the high frequency signal drive the mixer. Furthermore for future integration it is advantageous to implement a lower frequency mixer (simple topologies, low power consumption).

The output frequency of the synthesizer is calculated as

$$f_{OUT} = f_{OFFSET} + N \times f_{CHANNEL} = \\ = M \times f_{REF1} + N \times \left(\frac{M}{R \cdot X} \times f_{REF2} \right) \qquad (1)$$

The high – frequency loop offers a large offset frequency f_{OFFSET} (equal to $M \times f_{REF1}$), thus reducing the division ratio N of the low – frequency loop.

Regarding locking speed the locking procedure of the upper loop begins after the low – frequency loop output has settled to the new frequency. However, the settling time of the synthesizer depends mostly on the locking speed of the low – frequency loop. This is due to the fact that the reference frequency of the low – frequency loop is lower than the one of the high – frequency loop.

III. SYSTEM IMPLEMENTATION AND MEASUREMENTS

The system was implemented on a soft substrate with ε_r=6.15. It employees a parallel interface to program the N divider and uses discrete components to implement the upper and lower frequency loops. Discrete components give flexibility in the design of the system and allow for further improvement.

The active filter used at the high frequency loop and the 3rd order filter used at the low frequency loop are shown in Fig. 3(a) and Fig. 3(b) respectively. The loop filter determines settling time, phase noise and spurious levels. The output frequency of the lower loop VCO ranges from 1520 MHz to 1600 MHz with a 4 MHz step. It is divided by X = 2 to produce the LO input frequency of the SSB mixer. The 4850 MHz to 5050 MHz upper loop output has a step of 10 MHz, is divided by M = 5 and then down – converted by the LO signal to produce an IF signal of 210 MHz.

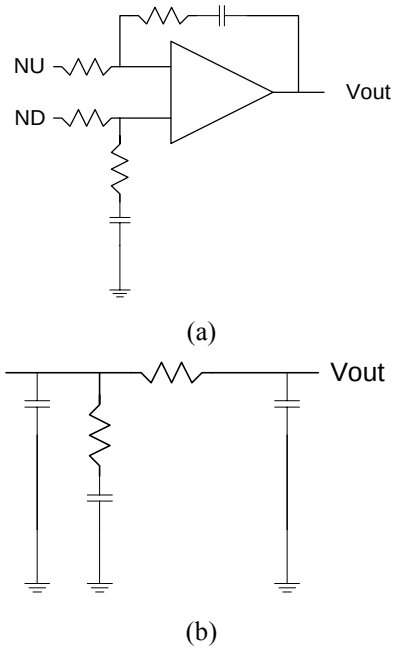

Fig. 3: Loop filters of the high (a) and low (b) frequency loops.

The IF signal is filtered and compared to the 210 MHz reference signal in the phase – frequency detector (PFD). The output spectrum measurement and the phase noise are presented in Fig. 4 and Fig. 5 respectively. The measured phase noise at the output of the synthesizer is -80 dBc/Hz at 300 kHz offset and -95 dBc/Hz at 1 MHz

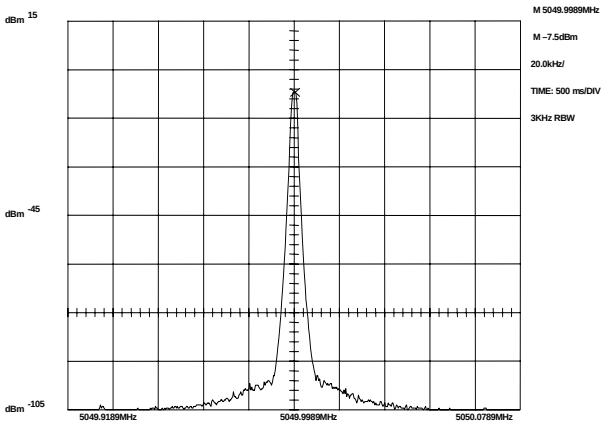

Fig. 4: Measurement of the output spectrum.

offset. The settling time is 900 μs and the output power is -7.5 dBm. The spurious levels are –98 dBc and -113 dBc at 4 MHz and 210 MHz frequency offsets, respectively. Although for lower jitter the phase noise spectral density, should be below -80 dBc/Hz up to a couple of hundred KHz frequency offset, this can be easily met by employing a better quality reference source.

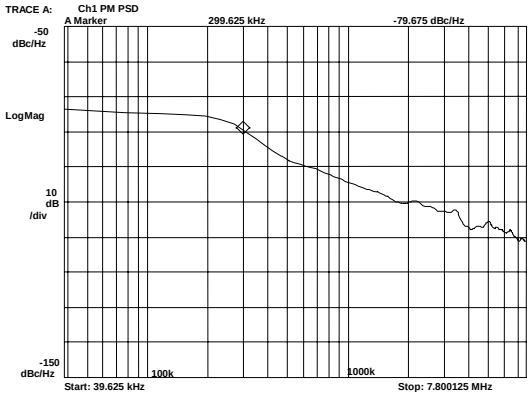

Fig. 5: Measurement of the phase noise.

Measurement results and a photograph of the implemented system are shown in Table I and Fig. 6 respectively.

Table 1: Measurement results of the dual loop synthesizer.

Specification	Achieved
Frequency range	4850 – 5050 MHz
Resolution	10 MHz
Phase noise @ 3 KHz	-75.72 dBc/Hz
Phase noise @ 300 KHz	-79.675 dBc/Hz
Spurious level @ 4 MHz	-98 dBc
Spurious level @ 210 MHz	-113 dBc
Settling time	900 μs

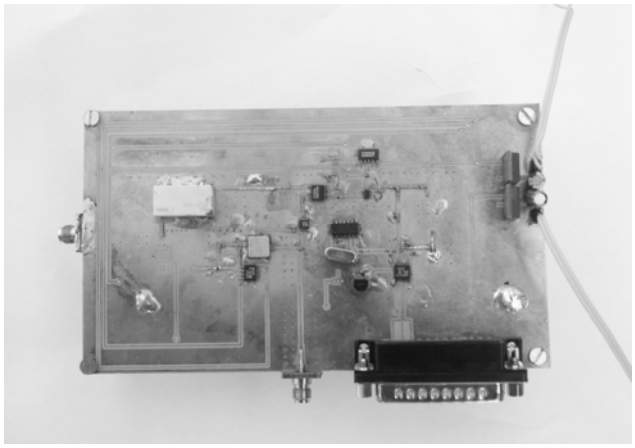

Fig. 6: A photograph of the implemented system.

IV. CONCLUSIONS

In this paper, the design and implementation of a 5 GHz frequency synthesizer is presented.

The dual – loop architecture achieves both good resolution and low phase noise and is thus suitable for 802.11a applications.

The low – frequency loop VCO generates signals in the range of 1520 MHz to 1600 MHz with a 2 MHz resolution, while the high – frequency loop VCO generates signals in the 4850 MHz to 5050 MHz range with a 10 MHz channel spacing.

The synthesizer is implemented with discrete components, offering an inexpensive, flexible design, with low overall output phase noise.

The divider of the high frequency loop is placed before the SSB mixer, which is required to operate in a much lower frequency range, compared to previously reported dual-loop architectures.

According to measurements, the synthesizer achieves a phase noise of -80 dBc/Hz at 300 kHz offset, with a settling time of about 900 μs and an output power level of -7.5 dBm. The spurious levels at the offset frequencies of 4 MHz and 210 MHz are -98 and -113 dBc respectively.

The measured phase noise is satisfactory for system integration in 5 GHz WLAN modems.

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