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Ultra-Wideband, Low-Power, Inductorless, 3.1–4.8 GHz, CMOS VCO

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Abstract A low-power, inductorless, UWB CMOS voltage controlled oscillator is designed in 0.18 μm CMOS technology targeting to a UWBFM transmitter application. The VCO is a Double-Cross-Coupled Multivibrator and generates output frequencies ranging from 1.55 GHz to 2.4 GHz. A low-power frequency doubler based on a Gilbert cell, which operates in weak inversion, doubles the VCO tuning range from 3.1 GHz to 4.8 GHz. The proportionality between the oscillation frequency and the bias current is avoided in this case for the entire achieved tuning range resulting in a low-power design. The selected architecture provides high suppression, over 45 dB, for the 1^{st} and 3^{rd} harmonics, while enabling high-frequency operation and conversion gain due to the unbalanced structure and the single-ended output. The proposed VCO draws 4 mA from a 1.8 V supply, it has a phase noise of −76.7 dBc/Hz at 1 MHz offset from the center frequency, while it exhibits a very high ratio of tuning range (43%) over power consumption equal to 7.76 dB.

Keywords Ultra Wideband FM (UWBFM) · Relaxation oscillator · CCO (current control oscillator) · Double-cross-coupled oscillator · Nearly sinusoidal oscillations · Frequency doubling

1 Introduction

Ultra-Wideband communications technology (UWB) aims to provide low-power, low cost, easy to implement and robust system solutions. It can be applied in today's short

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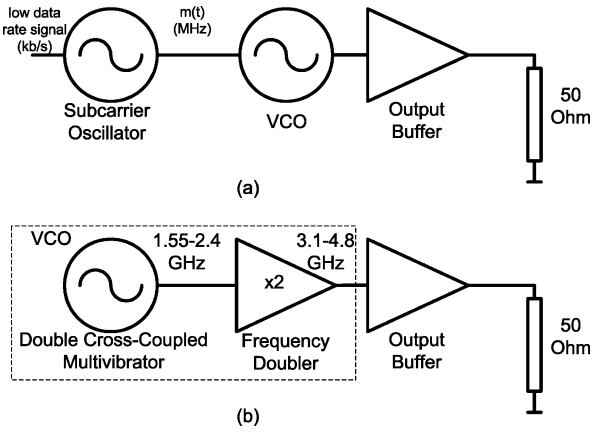

Fig. 1 (**a**) The complete UWBFM transmitter and (**b**) the proposed designed system

range, low or medium data rate communication devices, especially those used in wireless personal area network (WPAN) applications [1]. The design of wide bandwidth and low-power CMOS circuits becomes increasingly challenging due to the inherent limitations of CMOS technology such as low gain, low breakdown voltage, poor passive components, lack of accurate models, etc.

In [7] a novel UWBFM communication system was presented, promising lower complexity and power consumption when compared to the well known UWB impulse radio system. The transmitter consists of a wideband VCO which is FM modulated (high modulating index β_{FM}) by the output signal $m(t)$ of a subcarrier VCO. The latter is FM modulated, with low modulating index β_{FM}, by a low data rate signal as is shown in Fig. 1(a). This constant-envelope double frequency modulation technique enables the spread of the transmitted signal and multi-user operation. Phase noise performance is not so critical for a UWBFM system due to the non-coherent detection scheme of the receiver thus it can be relaxed in favor of lower power consumption; a maximum value of -70 dBc/Hz at 1 MHz offset was deemed satisfactory [7].

Aiming at the implementation of ultra wideband VCO circuits, the objective of this work is to develop an inductorless VCO of very low power consumption, high gain, wide range, with simple structure and constant output power over the entire tuning range that could form the main block of a UWBFM transmitter. The most important design goal is to achieve a very high ratio of tuning range over power consumption while meeting the phase noise requirement of a UWBFM system.

In this paper we propose an ultra wideband, low power, 3.1–4.8 GHz inductorless CMOS VCO shown in Fig. 1(b). This VCO is analyzed, designed and implemented in a 0.18 μm CMOS technology. It includes a Double-Cross-Coupled multivibrator which generates output frequencies between 1.55 GHz and 2.4 GHz by tuning a varactor and not the tail bias current, leading to a low complexity design with small die area and linear tuning range. A low-power frequency doubler based on a Gilbert cell which operates in weak inversion, doubles the VCO tuning range from 3.1 GHz to 4.8 GHz. Therefore, the proportionality between the oscillation frequency and the bias current is avoided for the entire achieved tuning range, resulting in a lower power design. The tuning range is doubled whereas the current consumption is not increased by a factor of two, as it holds for a standalone VCO/CCO, but it remains at the same

levels since the bias current of the frequency doubler which is added is very low. The latter implies that the sum of the bias current which is needed for the Double-Cross-Coupled multivibrator to maintain oscillations at 2.4 GHz and that of the frequency doubler is less than the bias current that would be needed for achieving VCO oscillations at 4.8 GHz without the use of a frequency-doubling mechanism. Furthermore, the unbalanced structure of the doubler enables high-frequency operation and conversion gain. A single-ended output is used in order to combine high-frequency performance with adequate conversion gain. We propose an analysis which demonstrates that, in weak inversion, as this imbalance increases the conversion gain of the frequency doubler increases as well. Finally, a wideband output buffer capable of driving 50 ohms is added.

The remainder of this paper is organized as follows: In Sect. 2 we describe in great detail the selected VCO topology and present the simulation results. The low-power frequency doubler analysis and simulation results are also given, whereas the design of the output buffer is discussed as well. In Sect. 3, the system simulation results are described and followed by a comparison with previously published work. Finally, in Sect. 4 we present our conclusions.

2 Circuit Design

2.1 The Design of a Source-Coupled Multivibrator as a Nearly Sinusoidal VCO

The Source-Coupled multivibrator has been used in the past in many Phase-Locked Loop (PLL) and Clock Data Recovery (CDR) applications. This oscillator topology generally offers wide tuning range and inductorless design. It exhibits better temperature stability of the oscillation frequency, when compared to ring oscillators, due to the single-stage design. However, its phase noise performance is poorer than that of ring oscillators and LC oscillators [17]. Tuning this VCO using a varactor provides a simple structure, constant output power over the full tuning range whereas the requirement for wide tuning range can still be met. Although CCOs promise high tuning range and linearity, their implementation becomes complicate due to the fact that as current is tuned in order to vary the oscillation frequency. Thus, an additional mechanism is needed for keeping the CCO output voltage constant, otherwise the oscillation frequency cannot be modulated. This mechanism deteriorates the oscillator phase noise performance and increases the power consumption. Moreover, the VCO modulation speed is limited, especially when the replica biasing technique is used [18]. A CCO can be transformed to a VCO if a voltage to current converter is used at the expense of further degradation of the VCO modulation speed and phase noise performance.

The Source-Coupled multivibrator is studied in [2] and [5] in order to accurately predict the oscillation frequency. In [15] a quadrature cross-coupled oscillator is studied, and the effect of coupling on the phase noise performance and the current consumption is presented. In [2] it is proved that this oscillator behavior can be either nearly sinusoidal-type or relaxation-type depending on the floating capacitance value, which implies that the poles of the transfer function of the oscillator are either complex conjugate to each other or both real. As the oscillation frequency is increased, the

floating capacitance must be decreased. This forces the poles of the transfer function of the oscillator to lay on the imaginary axis and as a result nearly sinusoidal oscillations occur whereas relaxation-type oscillations disappear. When the condition for oscillations is fulfilled, the roots have a positive real part and they are complex conjugate. For maintaining relaxation-type oscillations, the floating capacitance should be much higher than the related parasitic capacitances inside the oscillator core. Since the oscillation frequency is proportional to the ratio of the bias current over the floating capacitance, the bias current should be increased so that the desired frequency can be attained. Furthermore, in the case of relaxation-type oscillations the switching behavior of the MOS devices should be as good as possible such that the highest possible percentage of the bias current may pass via the floating capacitance and the maximum oscillation frequency can be achieved. This implies that the dissipated bias current should be used in the most efficient manner.

In [19] a double-cross-coupled multivibrator is used as relaxation-type current controlled oscillator (CCO). This ensures ideally 50% current consumption reduction due to the fact that the total bias current, which is given by only one tail current source (instead of two as is required in the classical source-coupled multivibrator), is redirected via the floating capacitance and the two cross-coupled pairs. Consequently, by using only one tail current source with the same current as in the classical multivibrator case, the same oscillation frequency can be achieved.

Another method which is used to increase the classical source-coupled multivibrator speed is to employ ECL buffers at the output of the oscillator instead of using classical source followers. Double-cross-coupled multivibrator designs with ECL buffers can be found in [16, 20, 21, 24, 25].

The selected oscillator topology is presented in Fig. 2. The VCO is used as a nearly sinusoidal oscillator, thus very good switching of devices M1–M4 is not needed, which allows for devices with smaller width. Two cross-coupled MOS pairs are used. As it is proved in [2], due to the transistors M1, M2 and the load resistances, the equivalent impedance which is seen at the capacitor nodes is given by the resistance R_p in parallel with an inductance L. This can be easily deduced by its small signal equivalent circuit, which is shown in Fig. 2. The values for R_p, L, and C_{TOTAL}, are obtained by solving the following equations (1) and (2). In (1), the predicted oscillation frequency ω_0 for nearly sinusoidal oscillations is given also.

$$\omega_0 = \sqrt{\frac{1}{LC_{\mathrm{TOTAL}}}}, \quad L = 2Rg_m^{-1}(C_{gs} + 4C_{gd}),$$

$$C_{\mathrm{TOTAL}} = C + C_{gs}/2 + 2 \cdot C_{gd}, \tag{1}$$

$$R_p = \frac{2R^2(4C_{gd} + C_{gs})\omega^2}{g_m(1 - g_m R)}, \quad \text{for } \omega \ll \tau_{gs}^{-1},\ \omega \ll \tau_{gd}^{-1}. \tag{2}$$

It is clear that R_p becomes negative for $g_m R > 1$ or equivalently when the start-up condition is met. As a result, the circuit in Fig. 2 behaves as a LC oscillator due to the transistors M1 and M2. The cross-coupled pair of M3 and M4 provides an additional negative resistance which equals $-2g_m^{-1}$ and it is connected in parallel with the negative resistance R_p. The advantage of this circuit, when it behaves as a second order

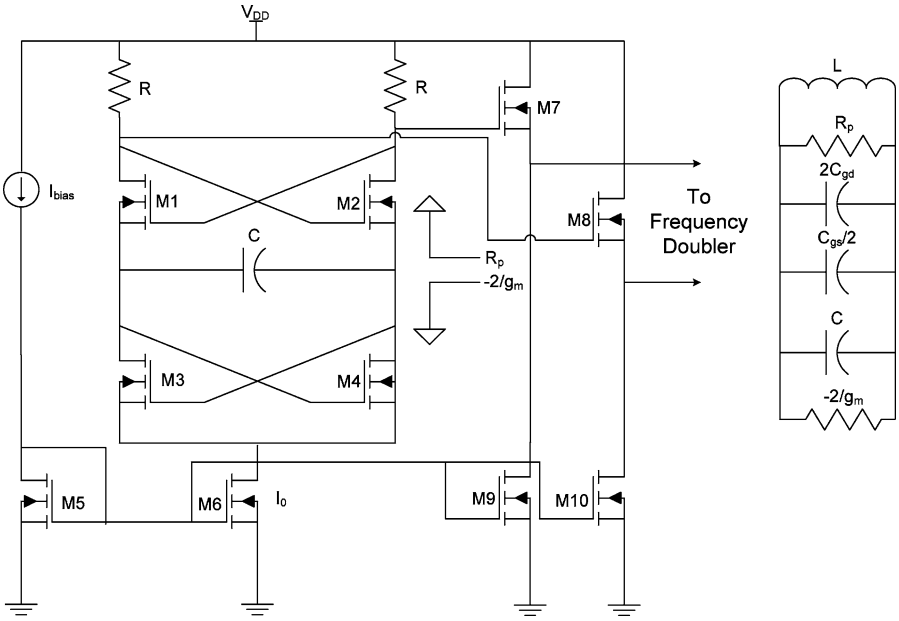

Fig. 2 A double source cross-coupled multivibrator and its small signal equivalent circuit

Table 1 Geometries of the devices of the VCO core as is shown in Fig. 2

	M1	M2	M3	M4	M7	M8
W/L (μm/μm)	10/0.18	10/0.18	10/0.18	10/0.18	10/0.18	10/0.18

oscillator, is that the start-up condition can be met at low power consumption, when compared to the basic source-coupled multivibrator. Bypassed source followers are used to buffer the oscillator output voltage, and thus, the speed of the VCO core is not limited. A varactor is used as a floating capacitor, which implies that oscillation frequency can be varied without modulating the oscillator output voltage. Consequently, an additional circuitry to keep the output voltage constant is not necessary, while the use of a voltage to current converter is avoided, reducing the power consumption.

As can be derived from (1), the lower the output resistance R is, the higher is the maximum achievable frequency. However, in this case the output voltage is reduced and the start-up condition becomes less easy to be met. Transient simulations results (Figs. 3, 4) showed that the previous requirements can be achieved when the output load of the oscillator is set to 270 ohms and the core devices are sized properly (Table 1) for the given bias current.

The drain-source voltage V_{DS} of the tail current source M6 is 125 mV and its saturation drain-source voltage $V_{DS,\text{sat}}$ is 90 mV. The gates of the transistors have the minimum width allowed by the technology (TSMC18RF). This ensures that the devices speed is maximized at the specified tail bias current of 1.2 mA. This bias

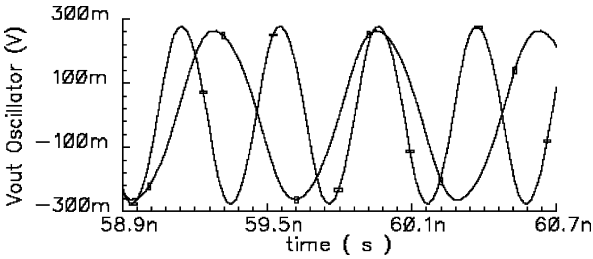

Fig. 3 Transient simulation results of the VCO differential output voltage at 2.49 GHz and 1.49 GHz

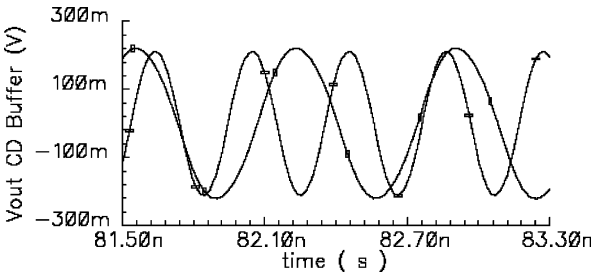

Fig. 4 Transient simulation results for the differential output voltage of the buffer at 2.49 GHz and 1.49 GHz

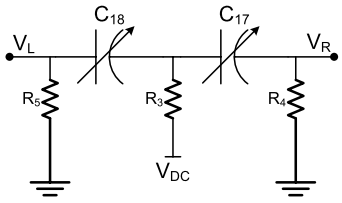

Fig. 5 The varactor biasing circuit

current is provided by a simple current mirror ($R_{\mathrm{BIAS}} = 7K$). As the gate width decreases the f_T of the MOSFETs increases for a fixed bias current. In other words, f_T is inversely proportional to the square root of the gate width at a fixed bias current. The same holds for the $V_{DS,\mathrm{sat}}$ of the MOSFET. This means that for setting M6 at a higher V_{DS}, the $V_{DS,\mathrm{sat}}$ of M1–M4 should be decreased (by increasing their gate widths). This cannot be a solution since in this way the speed of the VCO decreases. The common-drain buffers (M7, M8) are used to drive the frequency doubler that follows and set the gate bias voltage at its input. They consume 1.2 mA in total. The gate widths of the devices M7 and M8 are selected to be small enough so as not to load the VCO core. The differential output voltage of the oscillator is equal to 265 mV pk and the differential output voltage of the common-drain buffer is equal to 220 mV pk (when the frequency doubler is connected to the VCO buffer) at the oscillation frequency of 1.49 GHz. At 2.49 GHz the differential output voltage of the oscillator equals 276 mV pk and the differential output voltage of the common-drain buffer equals 211 mV pk. Consequently, the output voltage of the VCO remains nearly constant over the full tuning range. These transient simulation results are depicted in Figs. 3 and 4.

The biasing circuit of the diode varactor which was used for varying the VCO frequency is shown in Fig. 5. AC coupling capacitors are not included in order to obtain the maximum possible tuning range. It is well known that any capacitance in

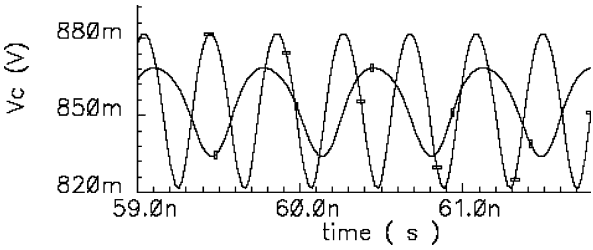

Fig. 6 Transient simulation result for the node *Vc* of the varactor at 2.49 GHz and 1.49 GHz

series with the varactor limits the tuning range and thus, in a realistic design very high capacitances are needed in order to overcome this problem (10 pF or higher). This leads to a large die area as well. Consequently, it was decided to implement the biasing circuit as is shown in Fig. 5, at the expense of about 320 μA which flows through R_4 and R_5. The dimensions of the two diode varactors are the minimum possible to keep the die area small also. The voltage difference between the nodes V_L and V_R at the minimum and maximum oscillation frequencies is shown in Fig. 6. It can be seen that it varies between 834 mV and 868 mV at 1.49 GHz, and between 820 mV and 880 mV at 2.49 GHz. Thus, when the DC tuning voltage varies from a voltage higher than 868 mV up to 1.8 V, the diode varactors are reverse biased and the VCO frequency does change. Frequency slightly changes for a tuning voltage lower than 868 mV, because the varactor junction capacitance is bias dependent even when it is forward biased. By simulating the *Y11* parameter of the varactor biasing circuit in Fig. 3 (an ideal DC voltage of 850 mV was applied at the nodes V_L and V_R via ideal inductors of 1 mH), the equivalent variable capacitance of this circuit was found to be 1.37 pF at a tuning voltage (*VDC*) of 0.65 V, 1.15 pF at 0.85 V and 0.51 pF at 1.8 V. If the varactors (reverse biased) were flipped, then the tuning voltage (*VDC*) should be varied between 0 V and 820 mV and the total capacitance variation would be less than that of the configuration presented in Fig. 3. The latter limits the VCO tuning range.

The equivalent inductance due to the upper cross-coupled pair is equal to 3.83 nH according to (1) ($g_m R$ is higher than one). If this is taken into account, together with the aforementioned values for the total capacitance of the varactor, then the minimum and maximum oscillation frequency can be calculated. The gate-source capacitance of the MOSFETs (M1, M2, M3, and M4) in the VCO core equals 0.019 pF and the gate-drain capacitance equals 0.00447 pF. The transconductance of the devices in the VCO core equals 4.18 mS. Using the small signal model of the oscillator presented in Fig. 2, the minimum oscillation frequency is found to be equal to 2.18 GHz and the maximum frequency is equal to 3.58 GHz. This small deviation from the simulated VCO frequency range can be explained by the fact that not all of the intrinsic capacitances of the small signal model of the MOSFET were taken into account. Moreover, the small signal analysis of this VCO (or the classical Source-Coupled multivibrator) predicts the oscillation frequency around the equilibrium point and not at the full operation region. However, the product $g_m R$ equals 1.12 and since it is higher than one, the start-up condition for oscillations is met. Thus, nearly sinusoidal-type oscillations are expected for a basic source-coupled multivibrator design according to the previous analysis (conjugate poles with positive real part). For the designed VCO, the

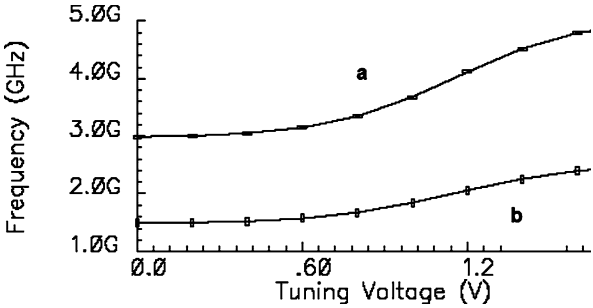

Fig. 7 PSS simulation result for the frequency versus tuning voltage characteristic for the (*a*) 2nd and (*b*) 1st harmonic component of the nearly sinusoidal multivibrator/VCO

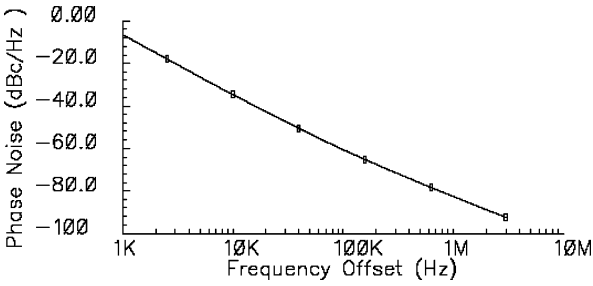

Fig. 8 Output phase noise of the VCO/multivibrator at 2 GHz versus frequency offset

upper cross-coupled pair (M1, M2) represents the virtual inductor (3.84 nH) and the equivalent parallel negative resistance R_p whereas the cross-coupled pair at the bottom (M3, M4) forms an additional negative resistance, which is in parallel with R_p. In this particular case there is not a positive resistance in series with the virtual inductor. Thus the parallel equivalent resistance which represents the losses of the tank can be assumed infinite, unless the series resistance of the varactor is taken into account. As a result, the absolute value of the parallel combination of the negative resistance $-2/g_m$, (formed by M3, M4) and the equivalent negative resistance R_p (for $g_m R$ higher than unity) is always smaller than the infinite positive resistance, which represents the losses of the tank. Consequently, the start-up condition is always met.

In Fig. 7 the PSS simulation results are shown for the frequency variation versus the tuning voltage for the first (Fig. 7(b)) and the second (Fig. 7(a)) harmonic component of the VCO. The second harmonic component of the VCO is generated by the frequency doubler that follows the VCO. PSS analysis of the VCO-Frequency Doubler system verifies this result, as will be shown in Sect. 3. The VCO frequency varies from 1.49 GHz to 2.49 GHz. However the linear region of the frequency versus tuning voltage curve is limited between 1.55 GHz and 2.4 GHz, which leads, due to the frequency doubler operation (Sects. 2.3 and 2.4), to a frequency range between 3.1 GHz and 4.8 GHz. The corresponding tuning voltage is between 0.6 V and 1.6 V. This gives a frequency to tuning voltage sensitivity equal to 1.7 GHz/V. The phase noise simulation performance of this VCO/multivibrator is shown in Fig. 8. At 1 MHz frequency offset from the carrier frequency of 2 GHz the phase noise is −82.7 dBc/Hz. This value is expected to be reduced at least by 6 dB due to the frequency-doubling mechanism which is provided by the frequency doubler. It could be generally improved by increasing the gate width of the VCO core devices at the expense of the VCO speed.

2.2 Analysis of an Unbalanced Differential Source-coupled Pair with MOSFETs Operating in Weak Inversion

A MOS transistor operates in the weak inversion region when the gate-source voltage is below the threshold voltage V_T, thus the effective gate-source voltage has a negative value. In this region, the total drain current is given by (3) and the transconductance by (4) [8]. The transistor enters the saturation region when the drain-source voltage becomes higher than the thermal voltage by a factor of three to four. In weak inversion, the MOSFET behaves similarly to a bipolar transistor, thus it obtains higher transconductance for the same bias current. This enables low voltage and low current MOSFET operation, which makes this regime favorable for low-power circuit design. As can be seen in (4), the transconductance is increased by increasing the drain bias current. However, if a higher value is desired, then the bias current should be increased and then the transistor may leave the sub-threshold regime and enter the saturation (strong inversion) regime. In order to keep the MOSFET operating in the weak inversion, while the bias current is increased, the gate width over length ratio should be increased, because in this way the saturation voltage of the transistor is decreased. In general, the saturation voltage of a MOSFET operating in weak inversion is lower than that of a MOSFET working in strong inversion. On the other hand, by increasing the gate width, the high-frequency performance of the MOSFET deteriorates, due to the increase of the device parasitic capacitances.

$$i_D = I_S \cdot \exp\left(\frac{v_{GS} - V_T}{n \cdot V_t}\right), \tag{3}$$

$$g_m = \frac{I_{D,\text{bias}}}{n \cdot V_t}, \tag{4}$$

where:

I_S is the specific current
V_t is the thermal voltage (25mV@ room temperature)
V_T is the MOSFET threshold voltage
v_{GS} is the total gate-source voltage (DC&AC)
n is the weak inversion slope factor
g_m is the transconductance
$I_{D,\text{bias}}$ is the drain bias current

$$I_S = 2 \cdot n \cdot \mu_n \cdot C_{ox} \cdot V_T^2 \cdot \frac{W}{L}. \tag{5}$$

The following equations describe operation of the unbalanced Source-Coupled pair operation in weak inversion (Fig. 9). The drain currents (Fig. 9) are given by (6), (7) and their difference by (8). Note that V_K is a virtual voltage which expresses the

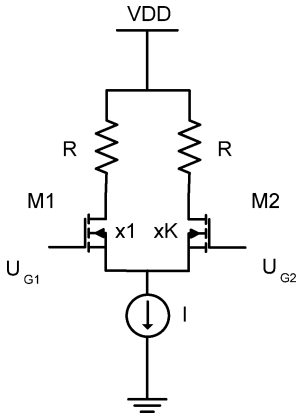

Fig. 9 Unbalanced source-coupled differential pair

difference in the widths of M1 and M2 in volts.

$$i_{D1} = I_{S,1} \cdot \exp\left(\frac{v_{G1} - v_{S1} - V_T}{n \cdot V_t}\right), \tag{6}$$

$$i_{D2} = I_{S,2} \cdot \exp\left(\frac{v_{G2} - v_{S2} - V_T}{n \cdot V_t}\right), \tag{7}$$

$$\underset{(\times K)}{i_{D2}} - \underset{(\times 1)}{i_{D1}} = I \cdot \tanh\left(\frac{v_d + V_K}{2 \cdot n \cdot V_t}\right), \tag{8}$$

where

$$v_{G1} = V_{G1} - \frac{v_d}{2}, \tag{9}$$

$$v_{G2} = V_{G2} + \frac{v_d}{2}, \tag{10}$$

$$K = \exp\left(\frac{V_K}{n \cdot V_t}\right), \qquad \frac{I_{S,2}}{I_{S,1}} = \frac{W_2}{W_1} = K, \tag{11}$$

$$v_D = A_d \cdot \cos \omega t, \tag{12}$$

$$\Delta V_{\text{out}} = -\frac{I \cdot R}{24 \cdot V_t^3 \cdot n^3}\Big[v_d^3 + 3 \cdot V_K \cdot v_d^2 + 3 \cdot v_d \cdot \left(V_K^2 - 4 \cdot V_t^2 \cdot n^2\right) + V_K \cdot \left(V_K^2 - 12 \cdot V_t^2 \cdot n^2\right)\Big]. \tag{13}$$

Equation (13) reveals that for an unbalanced MOSFET differential cell biased in the weak inversion regime, the differential output voltage includes the desirable 2nd harmonic component whereas the 1st and 3rd harmonic component are not canceled. Equation (8) will be silently used in the analysis in Sect. 2.4.

2.3 Analysis and Design of an Unbalanced Gilbert Cell with MOSFETs Operating in Weak Inversion

The circuit analysis when using bipolar devices is given in [10–12] (differential output) while it is proved that the differential output is free of the 1st and 3rd harmonic component. In [11], this principle is applied in a bipolar four-quadrant analog quarter-square multiplier and in [12], in a frequency mixer with a frequency doubler. MOS pseudologarithmic half-wave and full-wave rectifiers are presented in [10] based on the same principle. In [3, 14] the circuit shown in Fig. 10 is studied for both differential and single-ended output cases where the M1–M4 MOSFET devices are biased in the saturation regime. A measured output bandwidth of 4 GHz (from 1 GHz to 5 GHz) is achieved. To justify that 1st and 3rd harmonic components are canceled when M1–M4 are biased in weak inversion regime for either single-ended or differential output, we present the foregoing analysis. The latter is proved by (16) and (29). To our best knowledge, such an analysis has not been reported in the past. Moreover, the differential and single-ended conversion gain is calculated.

The currents I_L, I_R shown in Fig. 10 are given by

$$I_L = i_{D,1} + i_{D,3}, \tag{14a}$$

$$I_R = i_{D,2} + i_{D,4}. \tag{14b}$$

The differential output voltage is given by

$$\Delta V_{\text{out}} = R \cdot \left(i_{D,1} - i_{D,4}\right) - R \cdot \left(i_{D,3} - i_{D,2}\right). \tag{15}$$

Since the circuit shown in Fig. 10 is formed by two unbalanced MOSFET differential pairs (M2–M3 and M1–M4) we can substitute (8) into (15) and derive the following

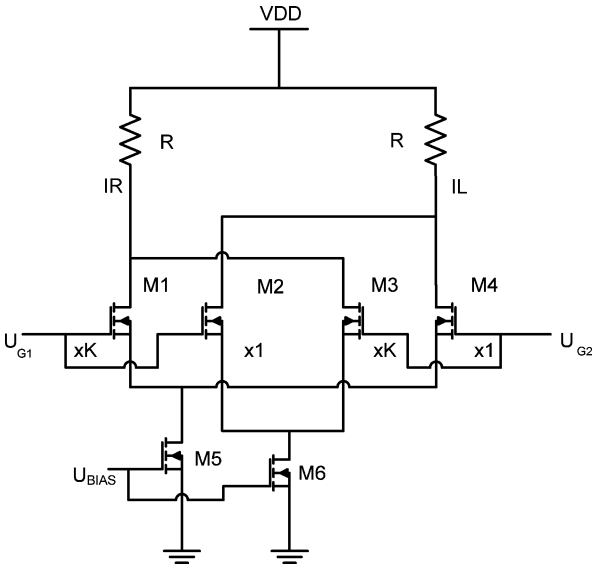

Fig. 10 Unbalanced Gilbert cell with MOSFETs in weak inversion regime

expression:

$$\Delta V_{\text{out}} \cong I \cdot R \cdot \left(\frac{V_K}{n \cdot V_t} - \frac{V_K^3}{12 \cdot V_t^3 \cdot n^3} - \frac{V_K \cdot A_d^2}{8 \cdot V_t^3 \cdot n^3} - \frac{V_K \cdot A_d^2}{8 \cdot V_t^3 \cdot n^3} \cos 2\omega t \right). \quad (16)$$

The differential conversion gain *DCG* is given by

$$DCG \equiv \frac{A_{d,\text{out}\,|\,2\omega}}{A_{d\,|\,\omega}} \cong \frac{I \cdot R \cdot A_d \cdot \ln K}{8 \cdot V_t^2 \cdot n^2}. \quad (17)$$

DCG is proportional to the bias current, the output load, the input signal amplitude, and the parameter $\ln K$.

The drain currents of M1–M4 are given by

$$\underset{(\times 1)}{i_{D2}} = \frac{I}{1 + \exp\left(\frac{-v_d + V_K}{n \cdot V_t}\right)}, \quad (18)$$

$$\underset{(\times 1)}{i_{D4}} = \frac{I}{1 + \exp\left(\frac{v_d + V_K}{n \cdot V_t}\right)}, \quad (19)$$

$$\underset{(\times K)}{i_{D1}} = \frac{I}{1 + \exp\left(\frac{-v_d - V_K}{n \cdot V_t}\right)}, \quad (20)$$

$$\underset{(\times K)}{i_{D3}} = \frac{I}{1 + \exp\left(\frac{v_d - V_K}{n \cdot V_t}\right)}. \quad (21)$$

From (19), (20) and (18), (21), it can be seen that V_K appears to behave as a part of the small signal input voltage. Moreover, when the unbalanced differential pairs formed by M1, M4 and M2, M3 are considered, the following observations can be made: In the first case, at the left input of the circuit there is a small signal input equal to $(-v_d - V_K)/2$ and at the right input there is a small input signal equal to $(v_d + V_K)/2$. This means that an equivalent differential small input signal exists equal to $\mp(v_d + V_K)/2$. In the second case the same holds, however the differential signal is now equal to $\mp(v_d - V_K)/2$. Since the gates of M1, M2 and M3, M4 are connected together, it can be assumed that either of these two different differential input signals is applied at the two inputs of the unbalanced Gilbert cell. The analysis continues assuming that a differential signal equal to $\mp(v_d + V_K)$ is applied.

$$\underset{(\times 1)}{i_{C2}} + \underset{(\times 1)}{i_{C4}} = I_{S(2,4)} \cdot \exp\left(\frac{V_{BE1} - \frac{v_d + V_K}{2}}{V_t} \right) + I_{S(2,4)} \cdot \exp\left(\frac{V_{BE2} + \frac{v_d + V_K}{2}}{V_t} \right) \quad (22)$$

or

$$\underset{(\times 1)}{i_{C2}} + \underset{(\times 1)}{i_{C4}} = I_{DC,(2,4)} \cdot \left(\exp\left(-\frac{v_d + V_K}{2 \cdot V_t} \right) + \exp\left(\frac{v_d + V_K}{2 \cdot V_t} \right) \right) \quad (23)$$

where:

$$I_{DC(2,4)} = I_{S,2} \cdot \exp\left(\frac{V_{GS} - V_T}{n \cdot V_t} \right). \quad (24)$$

By setting:

$$x = \frac{v_d + V_K}{2 \cdot V_t}, \tag{25}$$

using:

$$\exp(x) \cong 1 + x + \frac{x^2}{2}, \tag{26}$$

$$v_d(t) + V_K(t) = (A_d + V_K) \cdot \cos \omega t, \tag{27}$$

and (24) we derive:

$$\underset{(\times 1)}{i_{C2}} + \underset{(\times 1)}{i_{C4}} = I_{DC(2,4)} \cdot \left(2 + \left(\frac{A_d + V_K}{2 \cdot V_t}\right)^2 \cdot \cos^2 \omega t\right). \tag{28}$$

The single-ended output voltage is given by (28)

$$V_{\text{out}} = \left(\underset{(\times 1)}{i_{D2}} + \underset{(\times 1)}{i_{D4}}\right) \cdot R = 2 \cdot I_{DC(2,4)} \cdot R + I_{DC(2,4)} \cdot R \cdot \frac{(A_d + V_K)^2}{8 \cdot V_t^2 \cdot n^2}$$

$$+ I_{DC(2,4)} \cdot R \cdot \frac{(A_d + V_K)^2}{8 \cdot V_t^2 \cdot n^2} \cdot \cos 2\omega t. \tag{29}$$

The single-ended conversion gain *SECG* is given by (30) where it can be seen that as the parameter K increases, *SECG* increases as well.

$$SECG \equiv \frac{A_{\text{Single-Ended,Out}\,|\,2\omega}}{A_{d\,|\,\omega}} = I_{DC(2,4)} \cdot R \cdot \frac{(A_d + V_t \cdot n \cdot \ln K)^2}{8 \cdot V_t^2 \cdot n^2 \cdot A_d} \tag{30}$$

The final schematic of the frequency-doubling circuit which was used as an analog square multiplier is shown in Fig. 10. The gate width ratio K of the MOSFETs is set to 11.25 by selecting a gate width equal to 90 μm for the large transistors (M1, M3), and a gate width equal to 8 μm for the small transistors (M2, M4) the drains of which are connected to the output. The output load resistance is set to 1.5 kOhms. A polysilicon resistor was used due to its very good high-frequency performance (low parasitic capacitance). The channel length of all of the MOSFETs is set to the minimum, which equals 0.18 μm for the selected technology. This ensures that the transconductance g_m of the MOSFETs is maximum at a given gate width and bias drain current. The MOSFETs M1, M4 and M2, M3 are biased by the current sources M5 and M6, respectively, at 0.53 mA. The gate bias voltage V_{BIAS} of M5 and M6 is set to 0.8 V via a simple voltage reference (not shown here). The gate bias voltage V_G of M1, M2 and M3, M4 is set to 0.94 V via the output voltage of the common drain buffer of the oscillator. Their gate source voltage is forced in this way to be equal to 578 mV, whereas the threshold voltage in this case is 600 mV. This means that these MOSFETs are biased in the moderate inversion regime. In Table 2 the basic design parameters of the frequency-doubling circuit are given. The gate length of M5 and

Table 2 Basic design parameters of the frequency doubler shown in Fig. 10

MOSFETS	W/L	$V_{DS,\text{sat}}$
M1	90 µm/0.18 µm	60 mV
M2	8 µm/0.18 µm	67 mV
M3	90 µm/0.18µm	60 mV
M4	8 µm/0.18 µm	67 mV
M5	15 µm/0.5 µm	273 mV
M6	15 µm/0.5 µm	273 mV

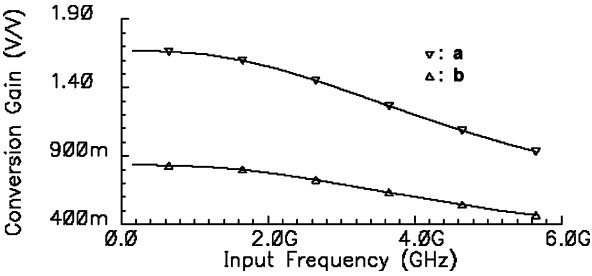

Fig. 11 (*a*) Single-ended Conversion Gain versus the frequency of the single ended input and (*b*) single-ended Conversion Gain versus the frequency if the differential input

M6 is increased as much as possible (0.5 µm) in order to limit their related thermal and $1/f$ flicker noise.

This can be clearly seen from (31), where the drain current noise spectral density of the MOSFETs is given, containing both thermal and flicker noise components [9]. Q_N is the net inversion layer charge and μ_{eff} is the effective mobility; both are calculated so that short channel effects are included (e.g. velocity saturation).

$$\overline{i_{nd}^2} = \overline{i_{nd,th}^2} + \overline{i_{nd,fl}^2} = |Q_N| \cdot \frac{4KT\mu_{\text{eff}}}{L^2} + \frac{K_f}{f}\frac{g_m^2}{WLC_{ox}^2}. \tag{31}$$

Thermal and flicker noise components of the biasing current sources of the frequency doubler deteriorate the total phase noise of the oscillator-frequency doubler system. This effect is added to the additional 6 dB increase of the phase noise of the system due to the frequency-doubling mechanism according to Leeson's model [13].

The Single-Ended Conversion Gain versus the differential input signal frequency is depicted in Fig. 11(a). It is equal to 0.735 V/V or −2.67 dB at the input signal frequency of 2.5 GHz. In Fig. 11(b) the Single-Ended Conversion Gain versus the single input signal frequency is given. The latter equals 1.47 V/V or 3.34 dB at 2.5 GHz. Figure 12 shows the Single-Ended output voltage in dB versus the input signal frequency for different offset values of (a) 0 mV, (b) 20 mV and (c) 100 mV. For obtaining this simulation result, an ideal DC voltage is connected at the left input of the circuit. For an offset of 20 mV the single-ended output voltage drops about 0.17 dB and for an offset of 100 mV it drops about 4 dB. The above simulation was performed in order to examine the robustness of our frequency doubler design against offset.

The $f_{3\text{ dB}}$ of the frequency doubler equals 3.26 GHz. This implies that a small output voltage modulation exists as the VCO frequency varies from 1.55 GHz to

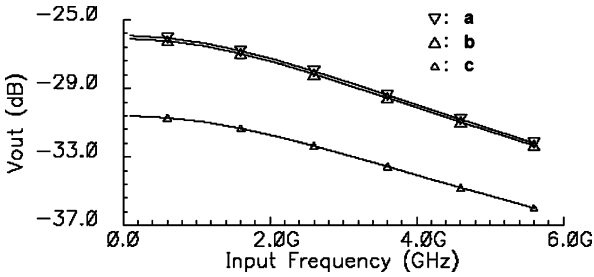

Fig. 12 Single-ended output voltage in dB versus the frequency of the input signal for different offset values of (*a*) 0 mV, (*b*) 20 mV and (*c*) 100 mV

2.4 GHz due to the frequency response of the doubler. It should be noted that the above simulation results were extracted assuming ideal input voltage sources without taking into account any source impedance (the output impedance of the oscillator buffer). The load at the output of the circuit is the input impedance of the output buffer of the system, and was not taken into account as well. All of these effects are highlighted in Sect. 3, where the full system (oscillator, frequency doubler and output buffer) is simulated.

Considering the single-ended output of this circuit the wideband design can be enhanced. This is due to the fact that the single-ended output (drain of M2, M4) is taken from the node of the circuit where the MOSFETs (M2, M4) have small gate widths. At the same time the increase in the gate width of M1 and M3 results in the increase of the conversion gain (single-ended and differential) at low input frequencies. On the other hand, if the differential output is considered, then due to the very large gate width of M1 and M3, the $f_{3\ \mathrm{dB}}$ of the circuit will be significantly decreased. When a single-ended output is considered then the $f_{3\ \mathrm{dB}}$ of the circuit is only set by the gate width of M2, M4. Consequently, the motivation here is to increase the conversion gain at low frequencies without influencing or limiting the wideband behavior ($f_{3\ \mathrm{dB}}$).

These two design parameters become independent when a single-ended output is considered. If the gate width of M1, M3 is decreased (compared to their size in the final design) whereas M2, M4 dimensions are kept constant, then a lower conversion gain (differential and single-ended) at low input frequencies is expected. In case that the differential output is considered then the $f_{3\ \mathrm{dB}}$ of the circuit will be lower than before (in the final design) due to the presence of M1, M3 (their gate width should still be higher than that of M2, M4) at the output. Thus, the differential conversion gain becomes comparable to the single-ended conversion gain of the final design or even smaller. At lower input frequencies (lower than 2.5 GHz) a differential output may be considered and the $f_{3\ \mathrm{dB}}$ of the circuit will be mostly limited by the gate width of M1, M3 which is the largest. In this way, the differential conversion gain is doubled at low frequencies. When $f_{3\ \mathrm{dB}}$ fulfills the desired specifications then this design option remains the best choice. The 4^{th} harmonic component and higher harmonics are present at the frequency doubler output. Yet, this does not cause a significant problem in the target application since these frequencies (6 GHz to 10 GHz) can be easily filtered out by the UWB antenna.

2.4 Output Buffer Topology

The output buffer (Fig. 13) consists of a wideband preamplifier, which drives an open-drain output cascode stage. The purpose of the preamplifier is to drive with sufficient amplitude swing the input of the output cascode stage up to the highest frequency of interest which in our application is 5 GHz or higher. Its power consumption will be determined by the required transconductance of the transistors for obtaining the desired bandwidth. It is advantageous, for wideband amplifier design, to bias the transistors at a current density near the region where the f_T is maximized. Moreover, by using small gate-width devices, the gate-source capacitance and the corresponding open time-constants are reduced.

The preamplifier is formed by a cascode stage (M2, M3) which is isolated from the input resistance R_S by an input common-drain amplifier (M1) and from the output capacitive load C_L by an output common-drain amplifier (M4). The output capacitive load C_L represents the gate-source capacitance of the output open-drain cascode stage (M5, M6). In the proposed system the output load of the frequency doubler is in the range of kOhms and represents the input resistance R_S of the output preamplifier. The input common-drain amplifier (M1) translates the high input resistance R_S to a much smaller one (the output resistance of M1). In this way the open time-constant, which corresponds to the gate-source terminals of the input transistor M2 of the cascode stage (M2, M3), is significantly decreased. The output common-drain stage (M4) of the preamplifier translates the high load resistance R_L of the preamplifier's cascode stage (M2, M3) to a much smaller resistance (the output resistance of M4). This results in the decrease of the open time-constant which corresponds to the capacitance C_L of the preamplifier. The resistance R_L should be high enough since it determines the voltage gain of the preamplifier.

For these reasons this circuit can meet the specifications of a wideband amplifier design with high input resistance. The voltage gain of the cascode stage of the preamplifier is decreased by the square of the voltage gain of a common-drain amplifier, if transistors M1 and M4 are biased at the same current. However, the current gain is significantly increased due to the presence of M1 and M4. The cascode configuration is used instead of a simple common source amplifier in order to eliminate the well known Miller effect. Similarly, the output stage of the buffer is chosen to be a cascode amplifier as well.

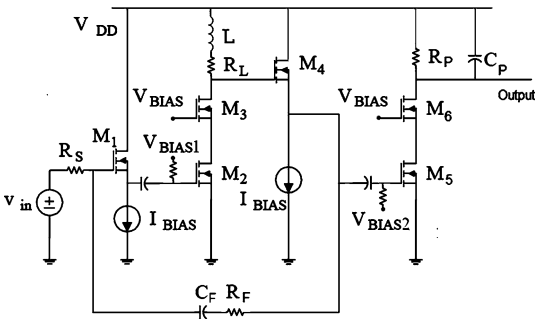

Fig. 13 Output buffer with resistive feedback and shunt-peaking inductor for extending $f_{3\,\mathrm{dB}}$

For applying proper biasing conditions to devices M1–M6, two DC block capacitors and bias resistors are used. The value of the DC block capacitors is kept as low as possible (0.5 pF and 1 pF). Diode-connected MOSFETs are used as simple voltage references. The load resistance R_L of M3 is set to 1 kOhm and the output pad capacitance C_P is set to 200 fF.

In order to increase the $f_{3\text{ dB}}$ of the output buffer, a shunt peaking inductor is used at the first cascode stage of M2–M3. The previously mentioned voltage modulation at the frequency doubler output can be limited by the use of the shunt peaking inductor. Thus, an overshoot may appear at the buffer gain plot at high frequencies, if the inductor value is high enough. In simulations, a 6.03 nH spiral inductor of the TSMC kit library has been used. In the actual layout design this inductor may not be included. A bondwire (1 nH/mm) can be used instead so that chip area remains small. The $f_{3\text{ dB}}$ of the output buffer with the shunt peaking inductor is increased by 12.9%.

Furthermore, resistive feedback is applied at the preamplifier (M1–M4) via R_F (Fig. 13). The latter is set to 1.6 kohms so that a voltage gain of approximately 1 V/V can be achieved for the preamplifier assuming that the source resistance R_S is equal to 1.5 kohms. A DC block capacitance C_F (0.2 pF) is also used in series with R_F such that the feedback network does not draw DC current. The effect of C_F in the frequency range of 3 to 5 GHz is small; the magnitude of $Z_{CF,RF}$ (the series combination of R_F and C_F) equals 1.621 kOhm and 1.607 kohm at 3 GHz and 5 GHz, respectively.

The simulated buffer output voltage under these conditions (shunt-peaking inductor and resistive feedback) is shown in Fig. 14 for an input voltage of 200 mV pk. The fact that the voltage amplitude increases with frequency is intentionally made by proper selection of R_F, C_F, and L. As the output voltage amplitude of the frequency doubler and the VCO decreases with frequency, the buffer voltage gain over the desired frequency range increases. This results in a relatively constant amplitude of the buffer output voltage when the two subsystems (VCO–frequency doubler and output buffer) are connected together. The buffer voltage gain for a source resistance of 1.5 kOhm is equal to 1.092 V/V (0.768 dB) at 5 GHz and it is equal to 0.815 V/V (-1.776 dB) at 3 GHz. The voltage amplitude at the output of the buffer equals -15.75 dB (or 163 mV) at 3 GHz and -13.21 dB (or 218.5 mV) at 5 GHz when a 200 mV pk input voltage is applied.

Finally, it should be noted that the last stage of the output buffer (M5, M6) is considered here as an open drain cascode stage. Thus the 50 Ohm load represents the measurement instrument characteristic impedance. If an RF chock inductor is

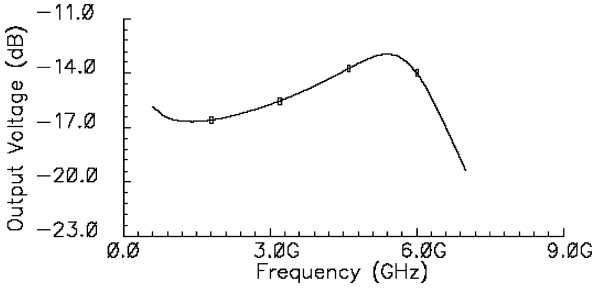

Fig. 14 AC simulation—Output voltage of the buffer with the shunt-peaking inductor versus frequency when resistive feedback is applied at the preamplifier

available (in case the chip is mounted on a PCB), then the instrument probe or the antenna could be directly connected at the buffer output through a DC block capacitor.

3 System Simulation Results

The performance of the full system is summarized in Table 3. The output voltage spectrum of the system is depicted in Fig. 15. It can be seen that the 1st and 3rd harmonic components are highly suppressed and that there is a very small voltage modulation of ±0.1 dB at the 50 Ohm load of the output buffer for the entire tuning range between 3.1 GHz and 4.8 GHz. In Fig. 16 the simulated phase noise performance of the VCO together with the frequency doubler is shown. Since the 2nd order harmonic frequencies of the proposed system are out of the operational frequency range of the UWB antenna (3.1–5 GHz), they are filtered out.

A performance comparison between the VCO presented in this paper and some other published results for wideband VCOs are given in Table 4. The figure-of-merit (FOM) factor in (32) is used to compare the VCO performance when phase noise and power consumption are taken into account. However, a better comparison among wideband VCOs, designed for UWBFM applications, can be made when the ratio of tuning range over power consumption is calculated. The latter can be derived by (33). Although the FOM of the proposed VCO is not of the highest ones, it should be

Table 3 Summary of schematic simulation results for the full system

VCO-FD-BUFFER	1st Harmonic	2nd Harmonic	3rd Harmonic
V_{OUT} (dB) @ $f_{2nd} = 2.988$ GHz	−83	−16.68 (146.6 mV)	−96.6
V_{OUT} (dB) @ $f_{2nd} = 4.939$ GHz	−79	−16.88 (143.2 mV)	−96

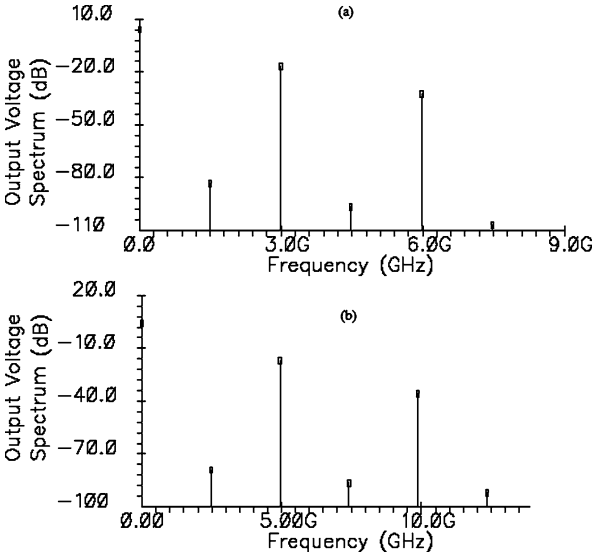

Fig. 15 Output voltage spectrum of the proposed system with the 2nd harmonic frequency (**a**) at 2.988 GHz and (**b**) at 4.939 GHz

Table 4 Performance comparison of wideband Voltage-Controlled Oscillators

References	Technology	Inductorless	Phase noise L (dBc/Hz) @ Δf offset	Oscillation frequency F_o (MHz)	Δf offset (MHz)	P_{DC} (mW)	Tuning range TR (%)	FOM	TR/P_{DC} (dB)
[15]	0.8 µm CMOS	yes	–	786.5	–	19.8	42	–	3.265
[24]	0.35 BiCMOS	no	−98.2	3,600	0.6	42	44.4	−157.53	0.241
[25]	0.35 BiCMOS	no	−113	4,300	0.6	36.5	46	−174.48	1.004
[27]	0.18 µm CMOS	yes	−66	745	2	5.4	28	−110.09	7.147
[4]	0.25 µm CMOS	no	−98.5	1,600	0.4	59	98	−152.83	2.203
[6]	0.18 µm CMOS	yes	−75	2,750	1	10.5	163	−133.57	11.909
[22]	0.18 µm CMOS	yes	−70	3,400	1	14	41.2	−129.16	4.687
[26]	0.18 µm CMOS	yes	−90	4,050	1	18.4	66.7	−149.50	5.593
[23]	0.18 µm CMOS	yes	−90.1	3,600	1	17	70.1	−148.92	6.152
This work	0.18 µm CMOS	yes	−76.7	3,950	1	7.2	43	−140.05	7.76

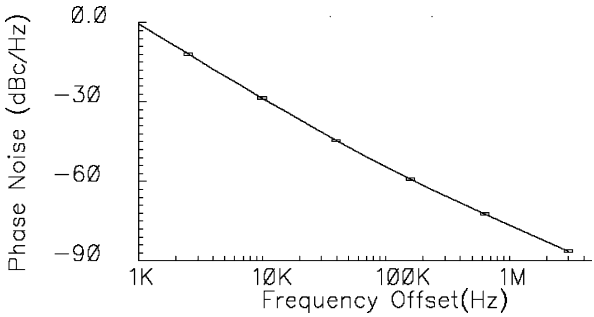

Fig. 16 Total phase noise at the output of the subsystem (VCO and frequency doubler) at 4 GHz versus frequency offset

stressed that the achieved ratio of tuning range over power consumption (TR/P_{DC} equals 5.972 or 7.76 dB), which has been set as the main design objective of this work, is comparable to the highest ones reported. Phase noise performance is satisfactory and meets the UWBFM transceiver requirement.

$$FOM = L(\Delta\omega)\left[\frac{\text{dBc}}{\text{Hz}}\right] - 20\cdot\log\left(\frac{\omega_0}{\Delta\omega}\right) + 10\cdot\log\left(\frac{P_{DC}\ (\text{mW})}{1\ \text{mW}}\right), \tag{32}$$

$$\text{Ratio of TR over}\, P_{DC},\ (\text{in dB}) = 10\cdot\log\left(\frac{TR\ (\text{in }\%)}{P_{DC}\ (\text{mW})}\right). \tag{33}$$

Frequency doublers are widely used for doubling the frequency of an available signal, yet this technique has not been proposed in this particular UWBFM application. Despite the use of the frequency-doubling mechanism, which deteriorates the phase noise of the VCO by at least 6 dBc/Hz, the achieved total phase noise performance satisfies the requirements of the UWBFM system.

Since the combination of the UWB VCO at lower oscillation frequencies and the use of the aforementioned frequency doubler leads to lower total power consumption, when compared to an autonomous VCO with oscillation frequencies between 3.1 GHz and 4.8 GHz, the applied technique was proved to be beneficial for meeting the design goals of the UWBFM application.

The presented VCO is tuned by employing a varactor instead of using variable current, as is traditionally preferred. The option of tuning the VCO by current would increase the circuit complexity, and deteriorate the phase noise performance due to both the employed tuning scheme and the necessary mechanism needed to maintain constant output swing. By appropriate filtering, phase noise performance can be improved, yet the die area is increased and the modulation speed of the VCO is dramatically limited. That, in turn, deteriorates the UWBFM system data rate. In addition, frequency stability is expected to be better, compared to that of ring oscillators.

Inevitably, the layout effect causes a small decrease in the oscillation frequency band and in the buffer output voltage especially at high frequencies due to the parasitic capacitances. The latter raises slightly the total output voltage modulation over the entire tuning range. In addition, a small decrease in the output voltage of the frequency doubler is expected. These three performance limitations were taken into account through the design procedure by inserting ideal capacitances of 10 fF at the critical nodes of the design (the oscillator differential output and the frequency doubler output). The buffer output stage is loaded by an ideal capacitance of 200 fF,

which represents the output RF PAD capacitance (80 fF, 50 μm × 50 μm) and ESD assembly.

In practice, all of the limitations caused by the layout effect can be fully compensated. The decrease in the oscillation frequency (approximately 250 MHz for parasitic capacitances of 10 fF) can be fully compensated by the bondwires inductance since the oscillator resistive load is placed in series with an inductance of at least 1 nH. Thus an inductive peaking load is achieved and the oscillation frequency is increased. The voltage drop at the buffer output at high frequencies (60 mV max) can be compensated by the inductor, which is placed at the 2^{nd} cascode stage of the output buffer and is implemented by a bondwire inductance. Further increase of this bondwire inductance can cause higher overshoot at high frequencies, which increases the output voltage swing as well and limits adequately the overall output voltage modulation.

4 Conclusions

In this work, a low-power, inductorless, UWB VCO was designed, operating at frequencies between 1.49 GHz and 2.47 GHz, followed by a low-power frequency doubler which was used to provide output frequencies between 2.98 GHz and 4.94 GHz. Nevertheless, the linear tuning range varies from 3.1 GHz to 4.8 GHz. The selected topology of the frequency doubler was analyzed in weak inversion regime and mathematical formulas were derived in order to examine and prove the related trade-offs in this region of operation. That allows for low-power design and high-frequency operation. A wideband output-open drain buffer was added in order to drive a 50 Ohm load.

The nearly sinusoidal behavior of a Source-Coupled-Multivibrator or a Double-Cross-Coupled-Multivibrator provides the advantage of inductorless design whereas the switching behavior of the transistors is not critical. An oscillator of this type can be easily transformed to a wideband VCO if the floating capacitance can be varied. Thus, power consumption can be saved since the VCO tuning is not achieved by varying the VCO bias current via a voltage to current converter. Moreover, tuning the VCO using a varactor, and not by modulating the bias current via a voltage to current converter, offers a high modulation speed. Current consumption is further improved since a circuitry to keep the VCO output voltage constant (like in CCOs) is avoided. It became clear that considering an UWB VCO, the proportionality between the oscillation frequency and the bias current is avoided for the entire achieved tuning range. This results in a low-power design, using a frequency doubler with very low power consumption. Therefore, a wideband, low-power frequency doubler design becomes an attractive solution since the total current consumption of the system (VCO and frequency doubler) can be less than the bias current that it would be needed for achieving VCO oscillation at the maximum desired frequency without the use of a frequency-doubling mechanism. The current consumption of the system is 10 mA (or 18 mW at 1.8 V), which is analyzed as follows: the VCO core consumes 1.1 mA, the common-drain buffer that follows consumes 1.2 mA and 0.32 mA are spent at the varactor branches. The frequency-doubling circuit and the output buffer draw 1 mA and 6 mA, respectively.

The proposed inductorless, low-power, wideband, CMOS VCO achieves a phase noise of −76.7 dBc/Hz at 1 MHz frequency offset, a wide tuning range of 43% and an output voltage modulation of ±0.1 dB over the desired frequency range, while it dissipates 7.2 mW from a 1.8 V supply. This VCO performance fulfills the requirements of UWBFM applications, where the phase noise performance is not so critical and thus it can be relaxed for achieving a higher ratio of tuning range over power consumption equal to 7.76 dB.

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