

This article was downloaded by: [University of Patras]

On: 04 April 2012, At: 03:03

Publisher: Taylor & Francis

Informa Ltd Registered in England and Wales Registered Number: 1072954 Registered office: Mortimer House, 37-41 Mortimer Street, London W1T 3JH, UK



International Journal of Electronics

Publication details, including instructions for authors and subscription information:

<http://www.tandfonline.com/loi/tetn20>

5-GHz fully differential multifunctional circuit

F. Plessas^a, A. Tsitouras^b & G. Kalivas^b

^a Department of Computer and Communication Engineering, University of Thessaly, Volos, Greece

^b Department of Electrical and Computer Engineering, University of Patras, Patra, Greece

Available online: 29 Mar 2012

To cite this article: F. Plessas, A. Tsitouras & G. Kalivas (2012): 5-GHz fully differential multifunctional circuit, International Journal of Electronics, DOI:10.1080/00207217.2012.669711

To link to this article: <http://dx.doi.org/10.1080/00207217.2012.669711>



PLEASE SCROLL DOWN FOR ARTICLE

Full terms and conditions of use: <http://www.tandfonline.com/page/terms-and-conditions>

This article may be used for research, teaching, and private study purposes. Any substantial or systematic reproduction, redistribution, reselling, loan, sub-licensing, systematic supply, or distribution in any form to anyone is expressly forbidden.

The publisher does not give any warranty express or implied or make any representation that the contents will be complete or accurate or up to date. The accuracy of any instructions, formulae, and drug doses should be independently verified with primary sources. The publisher shall not be liable for any loss, actions, claims, proceedings, demand, or costs or damages whatsoever or howsoever caused arising directly or indirectly in connection with or arising out of the use of this material.

5-GHz fully differential multifunctional circuit

F. Plessas^{a*}, A. Tsitouras^b and G. Kalivas^b

^aDepartment of Computer and Communication Engineering, University of Thessaly, Volos, Greece; ^bDepartment of Electrical and Computer Engineering, University of Patras, Patra, Greece

(Received 13 March 2011; final version received 26 December 2011)

This letter presents a multifunctional circuit realising the functions of oscillation, frequency multiplication and frequency division at 5-GHz. A theoretical and experimental description of the circuit is given. The injection signal, which is used to stabilise the oscillation, is at a sub- or super-harmonic of the oscillation frequency having a power level as low as -30 dBm. Calculations and measurements of the phase noise are reported which indicate a phase noise improvement. The implementation of the circuit exhibits a phase noise of -110 dBc/Hz at 100 KHz offset whereas the improvement depends on the relative noise of the injected signal.

Keywords: phase noise; injection locking; oscillator; frequency divider; frequency multiplier

1. Introduction

Configurable and reusable Radio-Frequency circuit blocks performing the functions of oscillation, frequency multiplication and frequency division have become an attractive alternative in terms of chip area, power consumption, cost and design time. One of the effective ways to build such a circuit is to use the injection locking technique. Injection locking is an approach to lock the state of a free-running oscillator by injecting an external signal of low phase noise. The frequency of the external signal must be within the operating frequency range of the oscillator at a fundamental, a sub-harmonic (sub-harmonic injection-locked oscillator (ILO)) or a super-harmonic of the required output frequency (super-harmonic ILO). Their reduced size and small consumption permits their use in applications such as active phased array antennas or in injection-locked phase-locked loops. Various architectures have been proposed for injection-locked frequency dividers (Rategh and Lee 1999; Cho, Tsai, Hung, and Liu 2008; Jin, Yu, Zhou, and Yan 2008), ILOs (Deng and Niknejad 2006; Mazzantia and Svelto 2006), and injection-locked frequency multipliers (Lin, Karasiewicz, Ciftcioglu, and Hui 2008; Hara, Sato, Murakami, Okada, and Matsuzawa 2009; Monaco, Borgarino, Svelto, and Mazzanti 2009; Wu, Chen, and Lo, 2009; Jang, Chen, Liu, and Juang 2010).

In this study, the design and experimental results of a novel multifunctional circuit are presented. The same circuit provides all the above-mentioned functions using the injection locking techniques. We extend our previous work, where we reported the experimental

*Corresponding author. Email: fotis.plessas@analogies.eu

results of a 5-GHz sub-harmonic ILO and self-oscillating mixer with a single-ended architecture and discrete components (Plessas, Papalambrou, and Kalivas 2008).

We use a $\div 2$, or a $\div 4$ sub-harmonic and an $\times 2$ super-harmonic signal, for stabilising the oscillation signal by injection. It should be mentioned that all three functions have not been previously implemented using the same function block.

A novel analysis is given to determine the phase noise performance of sub- or super-harmonic ILOs. Calculation results using the derived formula for the locking range and phase noise are presented. In addition, detailed experimental results are also provided. Section 2 describes the proposed circuit and presents the phase noise analysis, followed by implementation and measurement results in Section 3. In Section 4, summary and conclusions are presented.

2. Circuit and simulation

The proposed multifunctional circuit is composed of a differential Colpitts-based voltage controlled oscillator (VCO) and an enhanced biasing circuit as shown in Figure 1. The oscillator can function as: (a) free-running oscillator, (b) sub-harmonic ILO (frequency multiplier) or (c) super-harmonic ILO (frequency divider) depending on the applied signals at the input. The injection signal is applied at the collectors of Q_1 and Q_2 , whereas Q_5 and Q_6 serve as output buffers.

A new analytical formulation for the phase noise calculation of sub-harmonic ILOs is presented together with the equivalent model for the noise contribution. The analysis is based on the approach given in Chang, Cao, Mishra, and York (1997) for fundamental ILOs where a discrete MESFET VCO implementation has been used to validate the accuracy of the introduced model. In contrast to Chang et al. (1997), we study the noise

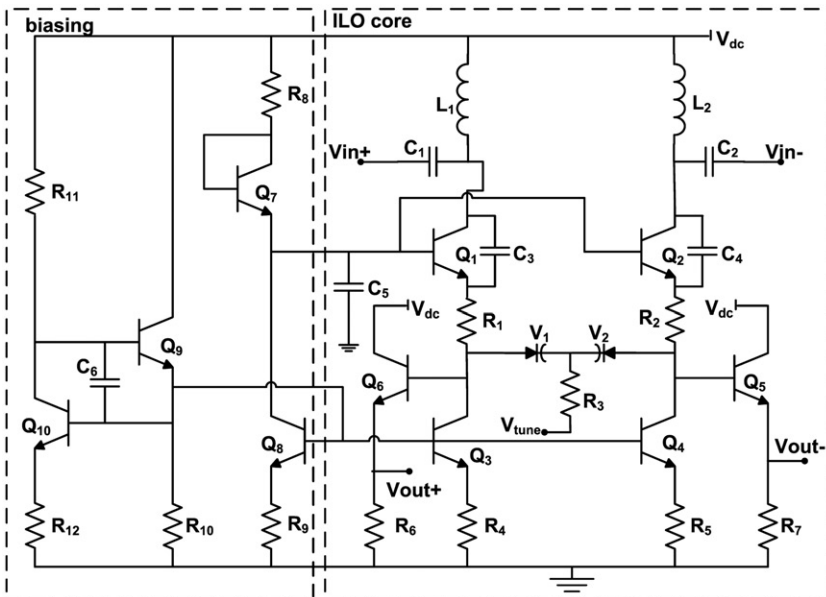


Figure 1. The schematic of the proposed multifunctional circuit.

behaviour of sub-harmonic injection-locked VCOs and the proposed theoretical analysis has been applied (for /2 and /4 sub-harmonic and ×2 super-harmonic injection locking) to a bipolar differential Colpitts oscillator implemented in a 0.5 μm SiGe BiCMOS technology.

As shown in Figure 2, the noise from the tank and the $-G_m$ cell can be represented as a noise admittance $Y_{noise} = G_{noise} + jB_{noise}$. The normalised admittance $Y_n = G_n + jB_n$ is defined with $G_n = G_{noise}/G_L$ and $B_n = B_{noise}/G_L$ where G_L is the oscillator load admittance in the free-running state. The terms G_n and B_n describe the in-phase (amplitude fluctuations) and the quadrature (phase fluctuations) component of the noise signal, respectively. In the absence of injection $-G_m$ (negative conductance) cancels G_T (loss of the tank) and therefore the phase noise is given by Chang et al. (1997):

$$|\delta\theta_0|^2 = \frac{|B_n|^2}{(2Q\omega/\omega_0)^2} \tag{1}$$

where ω_0 is the free-running frequency and Q the quality factor of the oscillator.

If the oscillator is injection locked to an external signal, the phase relationship between the oscillator and the injection source can be described as:

$$\frac{d\theta}{dt} = \omega_0 - \frac{\omega_0}{2Q} \rho \sin(\theta - n\psi_{inj}) - \frac{\omega_0}{2Q} B_n(t) \tag{2}$$

where θ , ψ_{inj} , are the instantaneous phases of the oscillator and the injection signal, respectively, ω_0 the free-running frequency, Q the quality factor of the oscillator, n an integer for the sub-harmonic factor and ρ the normalised injection strength. It should be noted that in sub-harmonic injection ($/n$), the oscillator locks onto the n th harmonic of the injection signal (called synchronising signal) introduced by the nonlinearities. If $V_{inj,n}$ is the amplitude of the n th harmonic and V_0 the amplitude if the free-running oscillator then $\rho = V_{inj,n}/V_0$.

If a steady-state solution can be found such that $d\theta/dt = n\omega_{inj}$ which indicates that the oscillator is synchronised to the injected signal. Under this assumption, it follows that:

$$\theta - n\psi_{inj} = \sin^{-1}[(\omega_0 - n\omega_{inj})/\Delta\omega_n] \tag{3}$$

where $\Delta\omega_n = (\omega_0/2Q)(V_{inj,n}/V_0)$.

The oscillation signal (f_{osc}) can be tuned using V_{tune} . However, when sinusoidal noise is added both to the oscillator and the injection signal, the instantaneous phase of the oscillator and the synchronising signal will be $\theta + \delta\theta$ and $\psi_{inj} + \delta\psi_{inj}$, respectively.

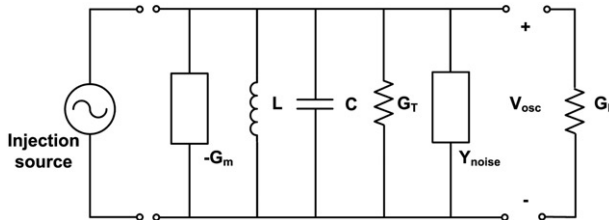


Figure 2. Oscillator model used for modelling the phase noise.

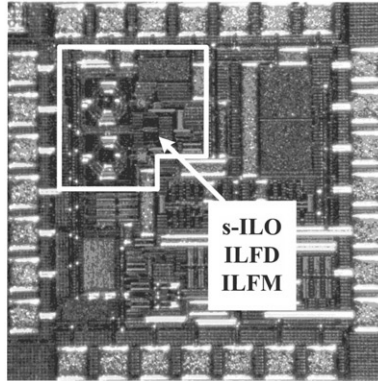


Figure 3. The microphotograph of the proposed circuit.

Neglecting the phase perturbation introduced during the harmonic generation process, (2) becomes the perturbed equation:

$$\frac{d\delta\theta}{dt} = -\frac{\omega_0}{2Q} \rho \cos(\theta - n\psi_{inj}) (\delta\theta - n\delta\psi_{inj}) - \frac{\omega_0}{2Q} B_n(t) \quad (4)$$

Next, the Fourier transform is calculated to obtain the expression for the total phase noise perturbation:

$$\delta\Theta = -\frac{B_n}{j\left(\frac{\omega}{\omega_{3dB}}\right) + \rho \cos(\theta - n\psi_{inj})} + \frac{n\rho \cos(\theta - n\psi_{inj})\delta\Psi_{inj}}{j\left(\frac{\omega}{\omega_{3dB}}\right) + \rho \cos(\theta - n\psi_{inj})} \quad (5)$$

where $\omega_{3dB} = \frac{\omega_0}{2Q}$

Multiplying by the adjoint $\delta\Theta^*$, the phase noise spectral density is given by:

$$|\delta\Theta|^2 = \frac{\left(\frac{\omega}{\omega_{3dB}}\right)^2 |\delta\Theta_0|^2}{\left(\frac{\omega}{\omega_{3dB}}\right)^2 + \rho^2 \cos^2(\theta - n\psi_{inj})} + \frac{n^n \rho^2 \cos^2(\theta - n\psi_{inj}) |\delta\Psi_{inj}|^2}{\left(\frac{\omega}{\omega_{3dB}}\right)^2 + \rho^2 \cos^2(\theta - n\psi_{inj})} \quad (6)$$

where $|\delta\Theta_0|^2 = \frac{|B_n|^2}{(\omega/\omega_{3dB})^2}$

To derive the above expression, it has been taken into account that the input noise is uncorrelated to the oscillator noise. We can easily derive the expression for the phase noise performance in super-harmonic injection after substituting n by $1/n$ in Equation (2) and therefore in Equation (6).

3. Measurement results

The main objective of the implementation was to verify the functionality of the circuit and the validity of the proposed analysis. For this purpose, the choice of the mature 0.5- μm SiGe BiCMOS technology was adequate. Figure 3 shows a microphotograph of the implemented (through the MOSIS fabrication service) circuit.

The tuning range is from 4.34 to 5.33 GHz as the control voltage is increased from 0 to 2 V, and the locking range is from 3.7 KHz to 5.5 MHz when the input power is varied

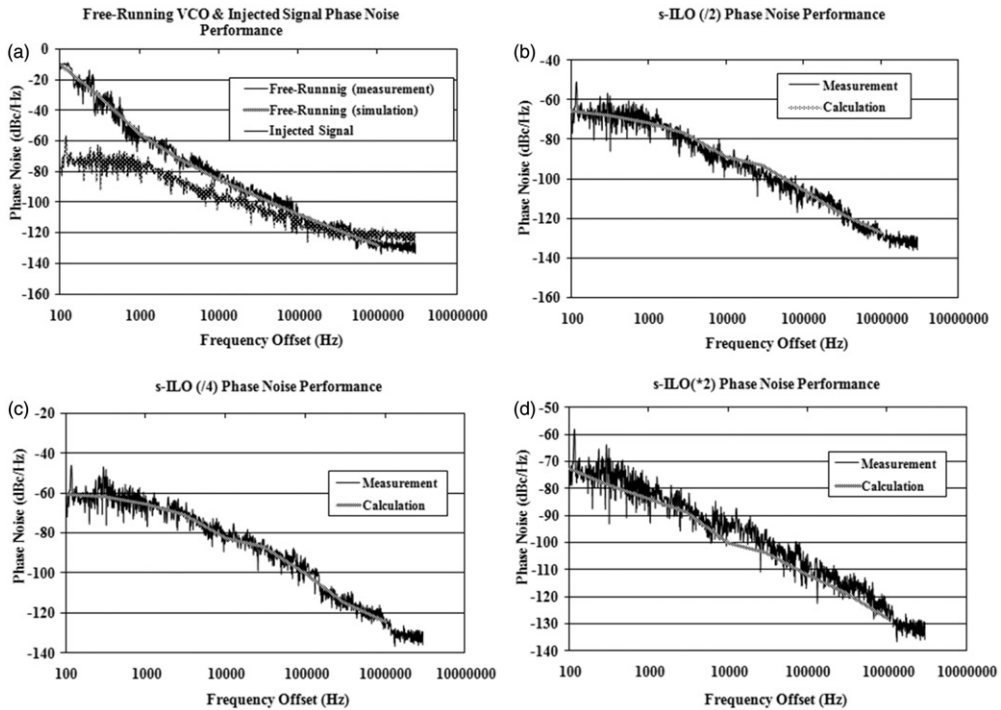


Figure 4. The phase noise performance of the proposed circuit.

from -45 to 0 dBm. The measured phase noise of the free-running oscillation signal was equal to -73.3 dBc/Hz at 5 KHz.

The measured, together with the computed phase noise profile, based on Equation (6), is shown in Figure 4. For the computation, the measured phase noise of the free-running oscillator and the measured phase noise of the 1.25 GHz reference signal have been used. After applying an injection signal at 1.25 GHz with a -50 dBm power level, a considerable phase noise reduction of the proposed circuit was measured at low frequency offsets as shown in Figure 4. The phase noise improvement is 16 dB at 1 KHz and 3 dB at 5 KHz (s-ILO /4). The calculations and measurements of the phase noise levels are in relatively good agreement. Further improvement of 21 dB at 1 KHz is obtained when a 2.5 GHz signal at -45 dBm is injected at the input (s-ILO /2). In the injection-locked frequency division mode, when a 10 GHz signal is applied, the phase noise of the output signal is 6 dB lower than that of the input signal and 32 dB lower than that of the free-running signal at 1 KHz (s-ILO *2). Finally, the measured power consumption is only 27 mW using a 3 V supply, and requires a 0.25 mm² total die area.

4. Conclusions

In this study, a multifunctional circuit was proposed realising a variety of different modes of operation including oscillation, fundamental, sub-harmonic and super-harmonic ILO. Experimental results demonstrated high performance operation in all modes of the

implemented circuit at 5 GHz. Furthermore, in order to stabilise the oscillator and improve the phase noise by 20 dB at 5-KHz a sub-harmonic of the free-running oscillation frequency at 1250 MHz with -50 dBm of power level was used. An injection signal at 2.5 GHz can be also applied giving a phase noise reduction of 20 dB at 1 KHz. When configured as a frequency divider by 2 (10 GHz input/5 GHz output), it improves the phase noise of the injected signal and the free-running VCO by 6 and 32 dB at 1 KHz, respectively. The power consumption for all the operations is only 27 mW. All the above demonstrate a novel, multifunction front-end component with low power consumption, suitable for integration in high-performance radio transceivers.

References

- Chang, H.C., Cao, X., Mishra, U., and York, R. (1997), 'Phase Noise in Coupled Oscillators: Theory and Experiment', *IEEE Transactions on Microwave Theory and Techniques*, 45, 604–615.
- Cho, L.C., Tsai, K.H., Hung, C.C., and Liu, S.I. (2008), '81.5–85.9 GHz Injection-locked Frequency Divider in 65 nm CMOS', *Electronics Letters*, 44, 966–968.
- Deng, Z., and Niknejad, A.M. (2006), '9.6/4.8 GHz Dual-mode Voltage-controlled Oscillator with Injection Locking', *Electronics Letters*, 42, 1344–1343.
- Hara, S., Sato, T., Murakami, R., Okada, K., and Matsuzawa, A. (2009), '60GHz Injection Locked Frequency Quadrupler with Quadrature Outputs in 65 nm CMOS Process', in *Proceedings of the Asia-Pacific Microwave Conference*, Singapore.
- Jang, S.L., Chen, J.J., Liu, C.C., and Juang, M.H. (2010), 'Injection-locked Frequency Tripler with Series-tuned Resonator in 0.13 μ m CMOS Technology', *Microwave and Optical Technology Letters*, 52, 1107–1110.
- Jin, J., Yu, X.P., Zhou, J.J., and Yan, T.T. (2008), 'Gigahertz Range Injection Locked Frequency Dividers with Band-width Enhancement and Supply Rejection', *Electronics Letters*, 44, 999–1000.
- Lin, Z., Karasiewich, D., Ciftcioglu, B., and Hui, W. (2008), 'A 1.6-to-32./4.8 GHz Dual-modulus Injection Locked Frequency Multiplier in 0.18 μ m Digital CMOS', in *Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Atlanta, GA, 15–17 June, pp. 427–430.
- Mazzantia, A., and Svelto, F. (2006), 'CMOS Injection Locked Oscillators for Quadrature Generation at Radio-frequency', *Microelectronics Journal*, 37, 1241–1250.
- Monaco, E., Borgarino, M., Svelto, F., and Mazzanti, A. (2009), 'A 5.2mW ku-Band CMOS Injection-locked Frequency Doubler with Differential Input/Output', in *Proceedings of the IEEE Custom Integrated Circuits Conference*, San Jose, CA, 13–16 September, pp. 61–64.
- Plessas, F., Papalambrou, A., and Kalivas, G. (2008), 'A 5-GHz Subharmonic Injection-Locked Oscillator and Self-Oscillating Mixer', *IEEE Transactions on Circuits and Systems II: Express Briefs*, 55, 633–637.
- Rategh, H., and Lee, T. (1999), 'Superharmonic Injection-locked Frequency Dividers', *IEEE Journal of Solid-State Circuits*, 34, 813–821.
- Wu, C.Y., Chen, M.C., and Lo, Y.K. (2009), 'A Phase-locked Loop with Injection-locked Frequency Multiplier in 0.18- μ m CMOS for V-Band Applications', *IEEE Transactions on Microwave Theory and Techniques*, 57, 1629–1636.