Phase noise performance of fully differential sub-harmonic injection-locked PLL

F. Plessas, F. Gioulekas and G. Kalivas

A fully differential sub-harmonic injection-locked phase-locked loop (PLL) that achieves improved levels of phase noise performance through the incorporation of injection locking and fully differential architecture is presented. Details concerning the design of each building block are given and the corresponding simulation results are presented. The system level architecture exploration is introduced together with the phase noise analysis. A physical implementation of the proposed design using a standard 0.5 μm SiGe BiCMOS process is also presented as a case study in order to prove the functionality as well as the overall performance. Phase noise improvement is 20 dB at 1 kHz when a sub-harmonic of the free-running oscillation frequency at 2.5 GHz with a −15 dBm power level is injected.

Introduction: Injection locking is an alternative approach to couple a noisy on-chip VCO to a clean reference. The phase noise of the injection-locked oscillator (ILO) tracks accurately the phase noise of the reference signal when the free-running frequency and the frequency of the reference (injected) signal are nearly the same. When the injection frequency is a sub-harmonic (n) of the oscillation frequency, the sub-harmonic injection-locked oscillator (s-ILO) increases the phase noise of the injected signal by 20log(n) within the locking range. The sub-harmonic injection-locked phase-locked loop (s-ILPLL) incorporates such an s-ILO whereas the injection signal is used as reference for the phase detector of the loop. Injection locking has been a flourishing research topic over past years, resulting in a wide range of proposed applications. In this Letter, we report an analytical model and an experimental exploration of a fully differential, sub-harmonic injection-locked phase-locked loop. We extend our previous work, where we reported the theoretical analysis and the testing results of a sub-harmonic injection-locked phase-locked loop, the implementation of which was based on a single-ended architecture and discrete components [1].

System design: In this Letter, as aforementioned, we extend our previous study [1] in two steps. First, we design a fully differential s-ILPLL; secondly, we implement the proposed scheme in an integrated instead of a discrete fashion as a proof-of-concept to demonstrate its functionality and validate the performed theoretical analysis. The external signal V_{inj} is applied to the injection port of the oscillator and to the external phase shifter. The latter sets up a quadrature phase difference between the two signals allowing the double balanced mixer/phase detector to work in the 'linear' region of its sinusoidal phase detection characteristic. The limiter is used to ensure that the power level of the injected signal does not exceed the power level at the output of the 5 to 2.5 GHz divider (Fig. 1*a*). It is well known that by employing sub-harmonic locking with a frequency ratio of 2:1, the phase noise inside the lock range ω_L is confined to $4S_{REF}(\omega)$, where $S_{REF}(\omega)$ denotes the phase noise of the injected signal. Previously reported works [2–4] treat the s-ILPLL as a PLL-locked oscillator in which an injection signal is applied. In contrast to these, we demonstrate that an s-ILPLL can be also considered as a PLL where the phase noise of an ILO replaces the phase noise of the VCO in the PLL noise expression. It can be easily proved that both models are equivalent concerning their mathematical descriptions.

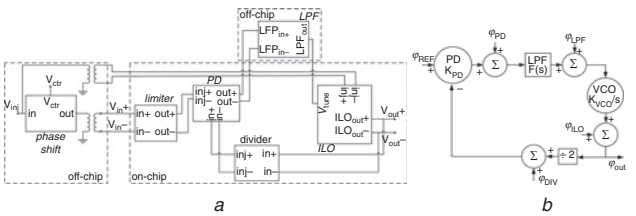

Fig. 1 *Block diagram of proposed s-ILPLL and model for noise analysis*

a Block diagram of proposed s-ILPLL
b Model for noise analysis

Component design: An SiGe HBT differential Colpitts oscillator was designed based on the single-ended Colpitts oscillator architecture. The simulated phase noise is depicted in Fig. 2*a*; the tuning range of the VCO is 4.9–5.1 GHz, i.e. 200 MHz, and the VCO gain (K_{VCO}) is 95 MHz/V. The phase noise of the sub-harmonic ILO locked at the second sub-harmonic frequency is given by [2]:

$$S_{ILO}(\omega) = \frac{4S_{REF}(\omega)(\omega_0/2Q(V_{OUT2}/V_{OUT}))^2\cos^2\varphi + \omega^2 S_{VCO}(\omega)}{(\omega_0/2Q(V_{OUT2}/V_{OUT}))^2\cos^2\varphi + \omega^2} \quad (1)$$

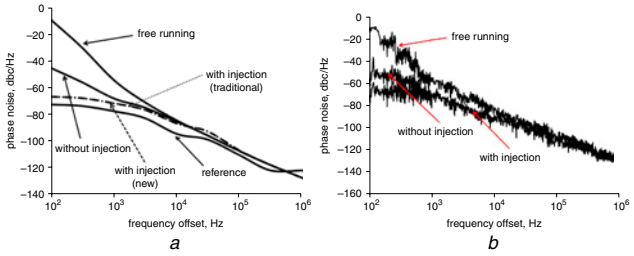

Fig. 2 *Calculated phase noise at output of proposed s-ILPLL using analysis considered in this study and measured phase noise performance with and without injection*

a Calculated phase at output of proposed s-ILPLL
b Measured phase noise performance with and without injection

where φ is the stationary phase difference between the oscillator and the second harmonic of the reference signal, ω is the offset carrier frequency, ω_0 is the free-running frequency, Q is the quality factor of the embedding network, V_{OUT} is the amplitude of the free-running signal and V_{OUT2} is the amplitude of the second harmonic of the reference signal at the output of the oscillator. $S_{VCO}(\omega)$ is the power spectral density of the phase noise of the free-running oscillator. We determined the phase noise spectral densities of the injection signal using a testing procedure and of the VCO by employing harmonic balance simulations. These results were used in (1) in order to calculate the total output phase noise at the output of the s-ILO. The locking bandwidth is 1.02 MHz.

Given that the frequency acquisition is obtained via the injection locking technique it is not necessary to employ a frequency detector within the proposed s-ILPLL scheme. In this case only a phase detection mechanism need be incorporated. The proposed architecture, used for phase detection, is based on a double-balance Gilbert-cell. The achieved (differential) K_{PD} is 350 mV/rad. A frequency divider has been incorporated to divide-by-two the frequency of the VCO's output signal. Consequently, the derived signal is compared to the external reference used for the purpose of the injection. The divide-by-two circuit is essentially a static master-slave D-latch.

We designed a limiter to ensure that the power level of the input signal does not exceed the power level at the output of the divider (Fig. 1*a*). The limiter is based on a cascode differential pair and the maximum differential output swing is 150 mV_{pp} at 2.5 GHz. To accommodate differential phase detector outputs and maintain the associated advantages, a differential version of the active proportional integral (PI) loop filter has been used. The combined functions of this filter concern the integration and the differential to single-ended conversion to provide V_{tune}. The time constants τ_1 and τ_2 of the loop filter were 36.7 and 0.9 ms, respectively.

Phase noise calculation and verification: Following the analysis presented in [1] and the linearised model of the s-ILPLL, shown in Fig. 1*b*, we arrive at the following expression for the spectral density of the phase noise at the output of the proposed s-ILPLL:

$$\begin{aligned} S_{ILPLL}(\omega) = {} & \frac{4S_{REF}(\omega)(\omega_0/2Q(V_{OUT2}/V_{OUT}))^2\cos^2\varphi}{(\omega_0/2Q(V_{OUT2}/V_{OUT}))^2\cos^2\varphi + \omega^2} \\ & \times |1 - H(\omega)|^2 \\ & + \frac{\omega^2 S_{VCO}(\omega)}{(\omega_0/2Q(V_{OUT2}/V_{OUT}))^2\cos^2\varphi + \omega^2} \\ & \times |1 - H(\omega)|^2 + 4S_{REF}(\omega)|H(\omega)|^2 \end{aligned} \quad (2)$$

where $S_{VCO}(\omega)$ and $S_{REF}(\omega)$ are the power spectral densities of the noise of the VCO and the injected signal (in units of rad^2/Hz), and $H(\omega)$ is the closed loop transfer function. The derived results obtained from the method described here are plotted in Fig. 2*a*. The reference frequency of the injected signal is set to 2.5 GHz. Phase noise data for the reference signal and the free-running VCO were collected from measurements. On

Downloaded 19 Sep 2010 to 150.140.254.62. Redistribution subject to IET licence or copyright; see http://ietdl.org/copyright.jsp

a first view, the derived formula (2) is different than the one derived in [2–4] but calculation results proved that the two equations are equivalent (dashed and dotted curves in Fig. 2*a*). Furthermore, the validity of (2) is confirmed by experimental measurements in the following Section. Finally, the output phase noise without injection (i.e. conventional PLL) is also depicted as reference. The proposed analysis is consistent with observations made by other authors in the literature [2–4], and can be used to characterise the phase noise performance of any ILPLL topology.

s-ILPLL integration and measurements: The main objective of the implementation addressed here is the verification of the functionality of the circuit and the validity of the proposed analysis. For this purpose the choice of the 0.5 μm SiGe BiCMOS IBM technology is adequate. Fig. 3 depicts the die microphotograph with an active area of 1.1 × 0.9 mm^2.

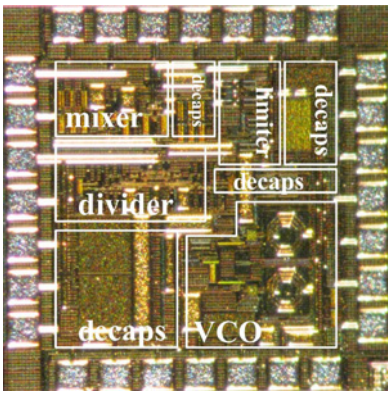

Fig. 3 *Microphotograph of proposed s-ILPLL*

Table 1: Comparison with recently published PLLs and s-ILPLLs

	Technology	Phase noise (dBc/Hz) at 500 kHz	Injected power (dBm)	Power consumption (mW)
This work	0.5 μm SiGe	−123(5 GHz)	−15	75
[2]	HEMT[1]	−82(18 GHz)	−10	–
[3]	90 nm CMOS	−123(5 GHz) [3]		38
[8]	GaAs[1]	−98(10 GHz)	−10	–
[7]	0.13 μm CMOS	−95(5GHz)	N/A[2]	31
[6]	0.5 μm SiGe	−110(5 GHz)	N/A[2]	231
[5]	0.25 μm SiGe	−115(5 GHz)	N/A[2]	287

[1] Discrete implementation, [2] PLL, [3] phase noise of the reference: −140 dBc/Hz

First, the s-ILPLL is measured under open-loop conditions, which means that the VCO frequency is directly adjusted by a steady voltage source. The loop locks at 90° where the phase detector output voltage is zero. Thus, K_{PD} is the first derivative of the voltage with relation to the phase difference evaluated at 90° and it is equal to 0.41 V/rad. The injected signal is then applied at the input (2.5 GHz at −15 dBm) and the phase noise of the s-ILO is measured, confirming the theoretical results. The next step refers to the implementation of the external loop filter by selecting the desired natural frequency ω_n (1500 rad/s), and the damping factor ζ (0.707). Consequently, the closed loop is employed and the stabilisation of the entire system has been proven. Fig. 2*b* shows the phase noise plots of the free-running oscillator and the output with and without injection. Measured performance data from the fabricated IC are consistent with the theoretical analysis. Table 1 summarises the performance of this and some prior work.

Conclusion: The successful realisation of a 5 GHz fully differential sub-harmonic injection-locked phase-locked loop in 0.5 μm SiGe BiCMOS technology has been presented. A sub-harmonic of the free-running oscillation frequency at 2.5GHz with −15 dBm of power level has been used, stabilising the oscillator and improving the phase noise by 20 dB at 1 kHz. The measured power consumption is 75 mW. This low-power level injection capability prompts integration of several s-ILPLLs sharing the same low-power reference signal while operating at different frequency bands. Thus, the proposed approach provides an attractive solution to implement frequency generators capable of covering different frequency bands simultaneously.

© The Institution of Engineering and Technology 2010
20 July 2010
doi: 10.1049/el.2010.1994
One or more of the Figures in this Letter are available in colour online.

F. Plessas (*Department of Computer & Communication Engineering, University of Thessaly, Greece*)

E-mail: fplessas@inf.uth.gr

F. Gioulekas (*Department of Computer Engineering & Informatics, University of Patras, Greece*)

G. Kalivas (*Applied Electronics Laboratory, Department of Electrical and Computer Engineering, University of Patras, Greece*)

References

1 Plessas, F., and Kalivas, G.: 'A subharmonically injected phase-locked loop for 5-GHz applications', *Microw. Opt. Technol. Lett.*, 2006, **48**, (11), pp. 2158–2162
2 Sturzebecher, D., Zhou, X., Zhang, X.S., and Daryoush, A.S.: 'Optically controlled oscillators for millimeter-wave phased-array antennas', *IEEE Trans. Microw. Theory Tech.*, 1993, **41**, (6/7), pp. 998–1004
3 Lee, J., and Wang, H.: 'Study of subharmonically injection-locked PLLs', *IEEE J. Solid-State Circuits*, 2009, **44**, (5), pp. 1539–1553
4 Razavi, B.: 'A study of injection locking and pulling in oscillators', *IEEE J. Solid-State Circuits*, 2004, **39**, (9), pp. 1415–1424
5 Osmany, S.A., Herzel, F., and Scheytt, J.C.: 'An integrated 0.6–4.6 GHz, 5–7 GHz, 10–14 GHz, and 20–28 GHz frequency synthesizer for software-defined radio applications'. Proc. 2009 Bipolar/BiCMOS Circuits and Technology Meeting, October 2009, Capri, Italy, pp. 39–42
6 Rogers, J.W.M., Cavin, M., Dai, F., and Rahn, D.: 'A ΔΣ fractional-N frequency synthesizer with multi-band PMOS VCOs for 2.4 and 5 GHz WLAN applications'. IEEE European Solid-State Circuits Conf., September 2003, Estoril, Portugal, pp. 651–654
7 Lee, J.-Y., Kim, K., Kwon, J., Lee, S.-C., Kim, J., and Lee, S.-H.: 'A 3.8–5.5-GHz multi-band CMOS frequency synthesizer for WPAN/WLAN applications'. IEEE Custom Integrated Circuits Conf., Sepember 2006, San Jose, CA, USA, pp. 377–380
8 Chang, H.C., Cao, X., Vaughan, M.J., Mishra, U., K., and York, R.A.: 'Phase noise in externally injection-locked oscillator arrays', *IEEE Trans. Microw. Theory Tech.*, 1997, **45**, (11), pp. 2035–2042

Downloaded 19 Sep 2010 to 150.140.254.62. Redistribution subject to IET licence or copyright; see http://ietdl.org/copyright.jsp