# Pseudo-FG technique for efficient energy harvesting

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A novel 2.45 GHz RF power harvester has been implemented in a 90 nm standard CMOS process. The proposed architecture reduces the threshold voltage ($V_{th}$) by employing a pseudo floating-gate (pseudo-FG) new technique and achieves better performance compared with other conventional rectifiers at 90 nm and 2.45 GHz, without additional fabrication cost. The system is initially optimised via a matching-boosting circuit, which has a dominant dual role. Extremely low power (−15.43 dBm) RF signals can be rectified and converted to 1.25 V DC.

*Introduction:* RF-powered devices are often used in applications where battery replacement is impossible so the RF power harvesting is an increasingly important technology. These devices require a power conversion circuit that can extract enough DC power from the incident RF wave. Rectifiers or RF-to-DC converters are used in these transponders where diodes or diode-connected MOS transistors are commonly used as far-field power extractors. Initially full- or half-wave bridge structures were used, but they are both constrained by the inherent diode/transistor forward-bias voltage drop, which affects the overall power efficiency. This negative impact becomes increasingly significant in the design of low-voltage power supplies. There are mainly three dominant topologies and the oldest was introduced by Dickson (as voltage-doubler, VD) [1]. Another common topology is the gate cross-coupled rectifier (GCCR or 'Favrat'), where two gate cross-connected transistors are used as switches so they do not suffer from voltage loss, due to the $V_{th}$ of transistors [2]. It is a modified version of the bridge full-wave rectifier, but lower voltage is required to turn the MOS fully on. The GCCR has a very good VCE and presents immunity to load changes. Finally fully cross-coupled structures (or negative voltage converters, NVCs) are present where all the MOSFETs act as switches [3]. The voltage at the input of the rectifier ($Q_t V_{RF}$) should be higher than the threshold voltage ($V_{th}$) for an effective rectification, where $V_{rf}$ is the received power and $Q_t$ is the total (loaded) quality/overvoltage boosting factor of the resonance circuit [2]. Hence, the necessity of low (LVT) or zero threshold (ZVT) transistors, or the use of threshold voltage reduction techniques is inevitable.

In this reported work, we have developed a novel rectifier circuit using a 90 nm CMOS process for 2.45 GHz RFID applications, an area in which only a few publications exist [4, 5]. The proposed RF front-end architecture includes a resonant voltage boosting network, which passively provides an adequate amplitude swing ($Q_t V_{RF}$) from a weak $V_{RF}$ signal, an $N$-stages rectifier, and a voltage limiter (regulator) for protection in a near-field situation. Additionally we introduce a novel modification of a basic GCCR cell, in order to reduce the threshold voltage $V_{th}$ of the required MOSFETs, and also to improve the overall conversion efficiency. Our booster-matching circuit plays a key dual role, to realise resonance (boosting) at 2.45 GHz and to inductively compensate ($L$-match) for the input impedance of the rectifier. The performance is verified by both simulation and measurement results.

*$V_{th}$ reduction methods:* Owing to the lack of power supply in passive tags the reduction of the 'dead zone' of the rectifier has to be performed using techniques that do not need additional power at the start up-state [3]. In such very low RF power conditions, MOS operation is in the sub-threshold region where the drain $I_{d,sub}$ and the reverse leakage $I_{leak}$ currents are related exponentially with the MOS diode voltage or with the very low RF voltage, unable to overcome $V_{th}$. An optimum design is achieved when one maximises $I_{d,sub}$ and minimises $I_{leak}$ simultaneously. This is the main reason for the usually bad performance of zero $V_{th}$ (ZVT) MOSFETs, owing to the rapid leakage of the reverse current when the transistor is 100% turned-off. Another trade-off exists between the need of small $V_{th}$ to handle very low voltages and the need of good turn-off of the transistor, which can be improved by large $V_{th}$. When the transistor exhibits very small threshold voltage its reverse blocking capability vanishes, because MOS is always on and large reverse current occurs. Otherwise the reduction of $V_{th}$ in standard CMOS rectifier designs is crucial.

Typically, the option of multiple threshold voltages is realised by adjusting the thickness of the $SiO_2$ or the doping profile in the channel, which complicates the process and circuitry, and adds cost. Alternatively, $V_{th}$ can be controlled by the bias voltage at the body (second/back-gate) terminal. A forward (or even zero) bias on the bulk–source junction ($V_{BS} \geq 0$) will cause a $V_{th}$ reduction in a reverse body effect, by the reduction of the depletion region [2, 4]. Another technique uses floating gate (FG) transistors, which imitate the operation of depletion mode transistors. Usually, a second control gate is used, which is responsible for the charge transferring control (to set $V_{th}$) after or during fabrication and is achieved by hot carrier injection through gate oxide or FN (Fowler-Nordheim) tunnelling [6]. However, FG-MOSFETs are not even a process option because, except cost, in nanometre lengths the gate oxide is very thin (a few Á) and a measurable gate current exists through $SiO_2$. So, gates cannot store charge that is needed in this method. Another drawback of these methods is usually the need of a battery for generation of bias or clocks, which is obviously unfeasible for passive RFIDs.

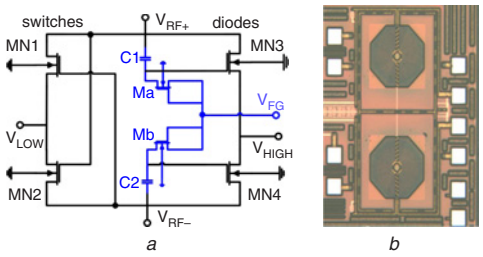


**Fig. 1** *Proposed GCCR (pseudo-FG cell), and microphotograph of proposed rectifier*

*a* Proposed GCCR
*b* Proposed rectifier

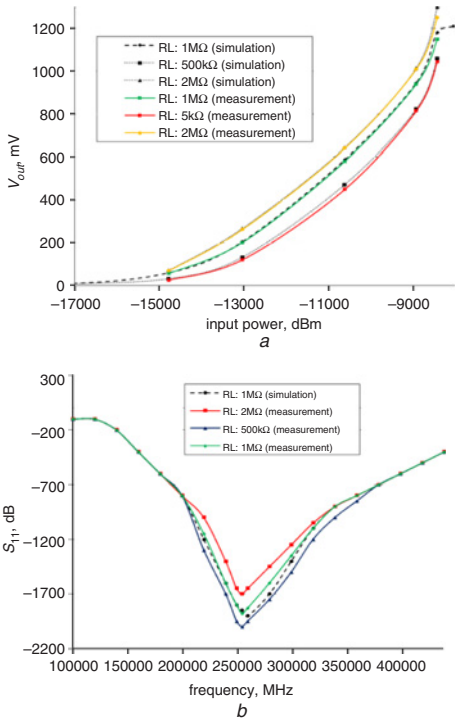


**Fig. 2** *Output DC voltage for different input power and output loads, and $S_{11}$ against frequency for different output loads*

*a* Output DC voltage
*b* $S_{11}$ against frequency

*Circuit design and results:* We relied on a 4-nMOS approach (transistors MN1, MN2, MN3, MN4), which can be transformed to a rectifier of $N$-stages, by connecting the $V_{LOW}$ of the first-stage to ground, while the RF signal plays the role of biphasic clocks. Capacitors to the RF +, RF − paths must be added, to avoid the flow of reverse currents [2]. Based on this basic GCCR cell, we introduce a modified one, the pseudo-FG, by the addition of two MOS diodes (Ma, Mb) and two capacitors ($C_1$, $C_2$) at the drain–gate connection path, as shown in Fig. 1*a*. The signal $V_{FG}$ that is essential for the reduction of threshold

can be formed by one efficient stage of a GCCR basic cell (MN1, MN2, MN3, MN4) using zero $V_{th}$ (ZVT) MOSFETs. A voltage is inserted in the drain–gate path of the diode connected transistors MN3, MN4 and if $V_{FG} = V_{th}$, then $V_s = V_d$ at MN3, MN4 [2]. Thus the threshold voltage of these MOSFETs is reduced according to the value of the $V_{FG}$ signal. This approach improves efficiency and reduces settling time and ripple. After optimisation, a four-stage GCCR pseudo-FG rectification circuit is presented and a prototype, shown in Fig. 1*b*, is fabricated able to generate 1.2 V of output DC. At a load of 1 MΩ we had 1.2 V from an incident RF signal of amplitude 125 mV (−8.06 dBm) corresponding to a distance from the source ($d$) of 55 cm, as shown in Table 1. Our efforts were focused on achieving a large VCE rather than a large power conversion efficiency (PCE). Large dimensions are used to sustain large currents (small $R_L$) needed in a large PCE [3–6]. For $V_{RF} = 125$ mV we obtained an improvement factor of 11.3% (from 943 to 1050 mV) with the contribution of the pseudo-FG signal to the reduction of $V_{th}$. It should be noted that the FG signal is almost stable for different frequencies and loads. Another real case rectification circuit is presented also, the GCCR-ZVT (all are ZVT now) in 20-stages. For an RF input of 53.5 mV (−15.43 dBm) with a load of 1 MΩ we had a stable 1.25 V DC output, an output power of 1.563 μW or a current of 1.25 μA, a VCE of 29.21% and a PCE of 5.46% at a range of 1.29 μm, as shown in Table 1. Measurements were focused on matching criteria and on the minimum power that is needed to create 1.2 V DC. Another constraint was the impedance matching between antenna, booster and rectifier. It is almost impossible to achieve best matching because a perfect matching circuit loses its boosting ability resulting in a poor $Q_t$, even capable of RF input attenuation [6]. Otherwise, tuning to the resonant frequency is more critical than the matching issue, which never ends in this pure nonlinear system. Because of this trade-off, we have detected a difference between the optimal matching frequency and the maximum $V_{out}$ frequency since the optimum $Q_t$ that maximises $V_{out}$ is achieved at a resonance frequency lower than 2.45 GHz. Simulation and measurement results for the output voltage against input power (Fig. 2*a*) and frequency are in good agreement. The input reflection coefficient in dB is −18.8 dB at 2.55 GHz (at 1 MΩ, Fig. 2*b*).

**Table 1:** Performance comparison

| [work]/L | STAGES/ TOPOL. | F (GHZ) | $P_t$- EIRP | $V_o$ (V) | $R_L$ (Ω) | PCE | VCE | S[a] (dBm) / $V_{in}$ (V) | d(m) | $Q_t$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Sim./90nm | 20/GCCR | This work | 0.5W | 1.25 | 1M | 5.46% | 29.21% | −15.43/53.5m | 1.29 | 2 |
| Exp./90nm | 4/GCCR | 2.45 | 0.5W | 1.2 | 1M | 1.00% | 64.36% | −8.06/125m | 0.55 | |
| [1] 0.5 μm | —/VD | 0.87 | 0.5W | 1.5 | 1M | 14.5% | — | −20.1/31.3m | 4.5 | — |
| [4] 90nm | 8/VD | 2.45 | — | 1.0 | 167K | 6.67% | 20.8% | −0.46/300m | — | — |
| [5] 0.5um | 6/VD | 2.45 | 4W | 1.2 | 1M | 37%[b,d] | — | −25.68[d]/73.5m | 6–12 | 3.2 |
| [7] 180nm | 24/VD | 0.90 | 0.32W | 1.8 | 0.47M | 4.43% | 17.66% | −8.06/125m | 1.10 | — |
| [6] 250nm | 36/VD | 0.92 | 4W | 2.0 | 1.32M | 32%[c] | 14.20% | −22.6/50m | 7–15 | 3.9 |
| [3] 180nm | 2/NVC | 0.95 | 4W | 0.5 | 0.25M | 23.5%[d] | — | −22.4[d]/33.86m | 21.6 | — |
| [8] 180nm | 4/VD | 0.92 | 4W | 1.0 | 0.5M | 5.14% | 28.63% | −14.1/62.37m | — | ~7 |

[a] input RF power, [b] $R_s = 300\Omega$, [c] at −8 dBm input power, [d] $G_s = 2$dBi

Table 1 presents a performance comparison with previously published harvesters. The proposed architectures are more efficient and robust compared to previously reported work, especially when taking into account the transmitted power $P_t$, the frequency of operation, the antenna gain $G_s$ and resistance $R_s$, and the load $R_L$. Given the absence of a widely accepted figure of merit, the comparison with previously published work might be misleading to the reader. Within this context, it is important to note that, to obtain the results reported here, real-valued antenna and load impedances have been assumed ($R_s = 50\ \Omega$ and $R_L = 1$ MΩ). Obviously, the PCE is proportional to $R_s$ but inversely proportional to $R_L$ [2]. The number of stages $N$ (very small in our case) has direct relationship to the die area and this also affects the results. The frequency of operation determines the free-space propagation loss (FSPL) and thus the range, whereas it provokes larger parasitic substrate capacitance losses [1]. Low transmitted power ($P_t$), which in our case is based on the very strict European (ETSI) regulations, also limits the coverage area. Finally, the proposed converter is fully integrated, so the achieved $Q_t$ is very poor (on-chip inductors) in contrast to the large total quality factors in designs with off-chip components.

*Conclusions:* A novel RF power harvester at 2.45 GHz has been implemented. With the aid of the proposed $V_{th}$ reduction techniques, improved performance is achieved using fabrication procedures in a 90 nm standard CMOS process, without additional cost. The fabricated four-stage pseudo-FG rectifier achieves a VCE of 64.36% and a PCE of 1% at 1 MΩ, for an input power of −8.06 dBm. The 20-stage GCCR-ZVT rectifier, generates a DC voltage of 1.25 V, for an input power of −15.43 dBm ($d = 1.29$ m) at 1MΩ load and achieves a PCE of 5.46% and a VCE of 29.2%. At 0.2 MΩ load, the corresponding values are PCE = 8.89%, VCE = 16.67%, and $d = 1.54$ m. Based on our measurements we conclude that the use of the proposed rectifiers in energising RFID tags or sensors appears to be realistic and effective.

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One or more of the Figures in this Letter are available in colour online.

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