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A 90 nm CMOS 15/60 GHz frequency quadrupler

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The design and characterisation of a 60 GHz frequency quadrupler implemented in a conventional 90 nm CMOS technology is presented. The proposed fully differential frequency quadrupler is formed by properly combining a 15 GHz to 30 GHz doubler, two 30 GHz amplifiers, a polyphase filter, a 30 to 60 GHz doubler and two 60 GHz amplifiers. The proposed design is based on a differential architecture and achieves enhanced characteristics in terms of harmonics rejection, bandwidth, power consumption and die area. Conversion loss of 9.3 dBm at 60 GHz with 1.1 dBm input power is achieved. The 3 dB bandwidth lies between 51.5 GHz and 61 GHz, while the total current consumption is 100 mA from a 1.2 V supply voltage for the fully balanced implementation.

Keywords: frequency doubler; frequency quadrupler; 60 GHz; LO amplifier

1. Introduction

Current and future communications require high data rate networks. Recently, part or complete 60 GHz based systems have been published in the literature, proposing single chip solutions implemented in several expensive technologies, like GaAs (Zirath, Masuda, Kozhuharov, and Ferndahl 2004; Kärnfelt, Kozhuharov, Zirath, and Angelov 2006; Gunnarsson et al. 2007; Kim, Song, Seo, and Kwon 2008) nP (Schefer 2002) and AlGaAs/InGaAs (Ito, Kishimoto, Morimoto, Hamada, and Maruhashi 2006). Other systems have been designed in SiGe technology (Liu, Ulusoy, Trasser, and Schumacher 2010),. Systems operating at 60 GHz are used today, among others, in data link applications for Gigabit Ethernet bridges, while the employment of 60 GHz systems is expected to be extended in the near future in wireless communication networks too. These call for the need to design such systems with common, low-cost CMOS technology (Kantanen, Holmberg, Karttaavi, and Volotinen 2008; Hara et al. 2009). However, the development of single chip solutions reveals many challenges due to the particular difficulties faced in their design. In particular, one of the major problems in such systems lies in the fact that they require an RF local oscillator at 60 GHz with low phase noise, low power consumption and sufficient output power level. Nevertheless, systems in this frequency range are difficult to meet these requirements (Zirath et al. 2004; Gunnarsson et al. 2007). In such a case a frequency quadrupler is the key component if a lower frequency, e.g. 15 GHz, PLL is to be utilised for easier phase lock and then having the signal multiplied up to 60 GHz. A tripler from 20 GHz to 60 GHz has also been reported in Chan and Long (2008).

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In most of these cases the conventional way for implementing the required millimeter-wave multipliers, employs the use of a nonlinear device and quarter-wave stubs for networks matching and for filtering the unwanted harmonics. This type of design relies on extensive EM analysis of matching structures and accurate device modelling, while the necessary stubs are approximately 2 mm long at 15 GHz leading to higher area consumption. In addition, as it can be deduced by researching the relevant technical literature, these implementations were found to be adopting the single ended approach with all the inherent disadvantages that characterise this technique.

In contrast to the above, in the current work a differential input, differential output 15 GHz to 60 GHz frequency quadrupler is reported, which is composed of a 15 GHz to 30 GHz doubler, two 30 GHz amplifiers, a polyphase filter, a 30 to 60 GHz doubler and two 60 GHz amplifiers, where the frequency doublers are implemented as double-balanced passive mixers. It is assumed that the frequency of 15 GHz is available through a quad output VCO, which is much easier to realise (with all the required advanced characteristics) in typical CMOS technologies. The quadrature outputs from a VCO can directly drive the frequency quadrupler in order to avoid the use of an input polpyhase filter. At 1.1 dBm input power, the quadrupler delivers 70 mV_{pp} to 50 Ohm output load at 60 GHz. The 3 dB bandwidth is between 51.5 GHz and 61 GHz, while the current consumption is 100 mA from a 1.2 V supply voltage. The quadrupler has been designed using the IBM CMOS 9 RF process where only a few implementations are given in the literature (Ferndahl, Motlagh, and Zirath 2004; Chan and Long 2008; Kantanen et al. 2008; Hara et al. 2009). Moreover, the CMOS implementation offers better compatibility with the preceding processing block, which in this case can be implemented in a conventional CMOS technology. Also, an active polyphase filter is used to produce the required four phases for the 30 GHz signal, which drives the 30 to 60 GHz doubler. The active filter gives the ability for external compensation of the phase shift if this diverges from the nominal value of 90°. Finally, as it will be analysed in the following paragraphs the proposed design compared with the aforementioned methods achieves better performance in terms of harmonics rejection, bandwidth, power consumption and die area.

2. Circuit design

2.1. *Architecture*

The conversion from 15 GHz to 60 GHz is based on the topology shown in Figure 1. It consists of two frequency doublers, one polyphase filter, gain amplifiers and the bias circuit. Following some trade-offs, several decisions must be taken for the optimum design of each block. First decision regards the type of the frequency doublers, where finally a passive double-balanced mixer has been chosen. Its main advantage in comparison to other topologies is its higher linearity. The disadvantages of this doubler is the requirement for a high level signal into the LO input while at the same time it exhibits high conversion loss. As a result, the output signal must be amplified significantly before it drives the next stages. Furthermore, it should be taken into account that this output will drive a second frequency doubler, which also requires high input level. Thus, two gain amplifiers have to be employed after the first frequency doubler. Specifically, two LO amplifiers have been used in cascade to amplify the doubler output resulting to a gain of about 15 dB. The next step is to double again the frequency from 30 GHz to 60 GHz. However, such a doubler would require two differential signals of the same frequency but shifted by 90°.

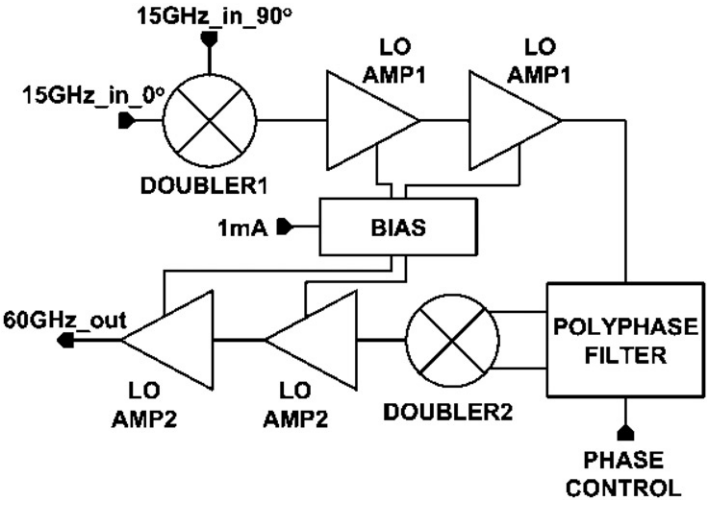

Figure 1. The full quadrupler topology.

Therefore, a polyphase filter is inserted before the doubler, providing two 90° shifted signals at 30 GHz frequency. To avoid the additional use of another polyphase filter before the first doubler, the two shifted signals are provided by the quad output VCO (not shown in this article), thus reducing the number of the polyphase filters needed. An active type of polyphase filter was used offering the capability for fine regulation in the case that the phase shift deviates from the required value. The second doubler follows the polyphase filter, resulting to a frequency doubling from 30 GHz to 60 GHz. Again, its output is considerably attenuated and must be amplified. Therefore two more gain LO amplifies are used to drive the signal, giving a final output of 70 mV_{pp}.

Each block used in the topology of Figure 1 is described in detail in the following paragraphs.

2.2. *Frequency doublers*

Typically, frequency doubling is implemented by multiplying two signals of the same frequency that are phase shifted by 90°, as represented by the equation:

$$\sin(\omega t) \times \cos(\omega t) = \frac{1}{2} \times \sin(2\omega t) \tag{1}$$

The multiplication of the signals is realised by a mixer. A double-balanced passive mixer has been chosen for performing the frequency doubling, as shown in Figure 2. This structure is more efficient with LO-IF and RF-IF isolations although it exhibits high conversion loss.

The mixer is mainly made of four switches that turn ON and OFF, generating the mixing process between the RF and LO ports. The IF signal is taken from the drain; the RF signal is fed to the source; and the LO signal is fed to the gate of the transistors. During the positive LO cycle, the RF signal is coupled to the IF port with positive phase, whereas

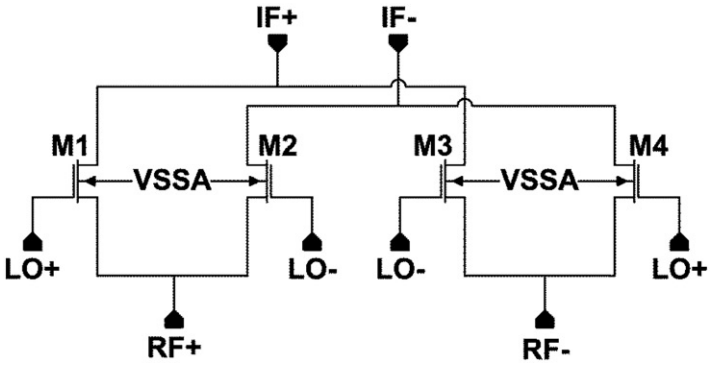

Figure 2. The frequency doubler.

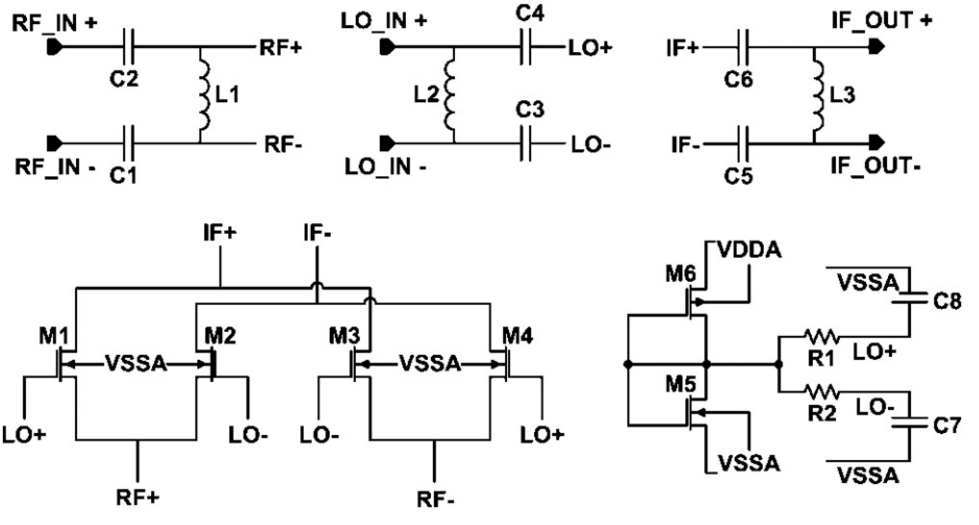

Figure 3. The complete schematic of the frequency doubler.

during the negative phase it is inverted at the IF. For an optimum IF signal transfer, the LO signal is applied along with a dc gate bias around the NMOS threshold voltage and thus only a MOSFET voltage reference has been employed. Since the input signal is differential, the RF and the LO ports are driven through an LC matching network to maximise the RF and LO voltage amplitude presented to the mixer. A similar network is used at the IF port also. The complete schematic diagram is shown in Figure 3.

The problem with this type of passive doublers, as aforementioned, is that they exhibit high conversion loss, with the result that the IF signal is considerably attenuated compared to the RF input. This situation is getting worse if the LO signal has small amplitude. For this reason, all inputs must preserve a high amplitude level. In order to reach the ideal value of −9.943 dB (Komoni, Sonkusale, and Dawe 2008) for the voltage conversion gain, the device performing the multiplication should not introduce any undesired output frequencies owing to its nonlinear characteristics or its high frequency limitations.

Table 1. 15 to 30 GHz frequency doubler.

Component	Value	Component	Value	Component	Value (um/nm)
C1	700 fF	C8	700 fF	$(W/L)_{M1}$	260/100
C2	700 fF	L1	384 pH	$(W/L)_{M2}$	460/100
C3	700 fF	L2	384 pH	$(W/L)_{M3}$	260/100
C4	700 fF	L3	204 pH	$(W/L)_{M4}$	460/100
C5	700 fF	R1	3.15 kOhm	$(W/L)_{M5}$	30/100
C6	700 fF	R2	3.15 kOhm	$(W/L)_{M6}$	360/100
C7	700 fF				

Table 2. 30 to 60 GHz frequency doubler.

Component	Value	Component	Value	Component	Value (um/nm)
C1	700 fF	C8	700 fF	$(W/L)_{M1}$	260/100
C2	700 fF	L1	128 pH	$(W/L)_{M2}$	460/100
C3	700 fF	L2	173 pH	$(W/L)_{M3}$	260/100
C4	700 fF	L3	70 pH	$(W/L)_{M4}$	460/100
C5	700 fF	R1	3.15 kOhm	$(W/L)_{M5}$	30/100
C6	700 fF	R2	3.15 kOhm	$(W/L)_{M6}$	360/100
C7	700 fF				

Furthermore, there is a trade-off between noise figure (NF) and required LO drive. The large W/L ratio will lead to low NF, however the required LO gain, power dissipation and area of the following LO amplifiers increase, due to larger transistor capacitances. The values of the components that have been employed in this design are shown in Tables 1 and 2 for the 30 and 60 GHz doublers, respectively. The LO transistors are biased in the vicinity of the threshold voltage by providing bias voltage to the switching transistors gates through the R1 and R2 resistors.

Unmatched pairs have been used ($W_{M2}/W_{M1} = 46/26$) in order to optimise the phase and the amplitude difference between IF+ and IF− outputs. The input and output signals of the 15 GHz to 30 GHz doubler and the S-parameter simulation results are shown in Figures 4 and 5, respectively. The corresponding simulation results for the frequency doubler from 30 GHz to 60 GHz are shown in Figures 6 and 7, respectively.

The active input matching was evaluated by simulating the small-signal parameters; S11 is found to be below −10 dB from 6 to 45 GHz.

2.3. *Polyphase filter*

The required generation of two 90° shifted phases from one signal with frequency 30 GHz is performed via a polyphase filter (Behbahani, Kishigai, Leete, and Abidi 2001). This is a circuit generating quadrature signals by using a differential one. The passive polyphase filter in Figure 8 has as input two sine signals of the same frequency, with equal amplitude and phase difference of 180° as depicted in Figure 9. The outputs of the polyphase filter are

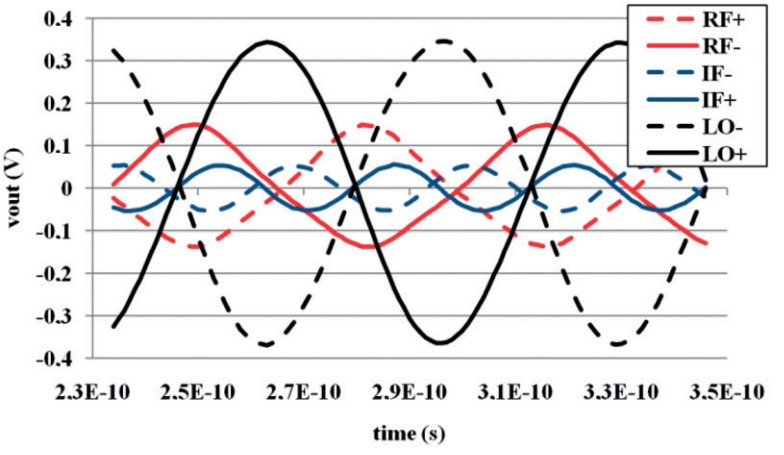

Figure 4. 30 GHz doubler transient simulation results.

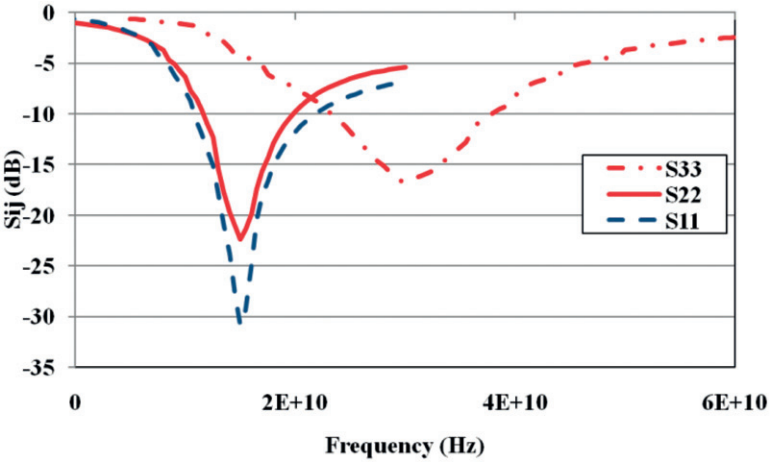

Figure 5. 30 GHz doubler input/output matching.

four sine wave signals with the same amplitude and 90° phase shift between each output respectively, as depicted in Figure 10. The required operating frequency of the polyphase filter in this topology is 30 GHz, which makes the design very challenging. The most fundamental way to design a polyphase filter is by employing resistors and capacitors. However, in this case, every mismatch, element tolerance or asymmetry in the signals and the design, affects the output which may easily result to nonquadrature signals. Thus, it would be preferable that the passive topology be replaced by a most efficient design, able to give a small control to its operation, compensating the tolerances of the output signals.

The polyphase filter utilises the concept of the *RC* networks and the properties of the integrators which give 45° phase at their output signal. Accordingly, in order to achieve

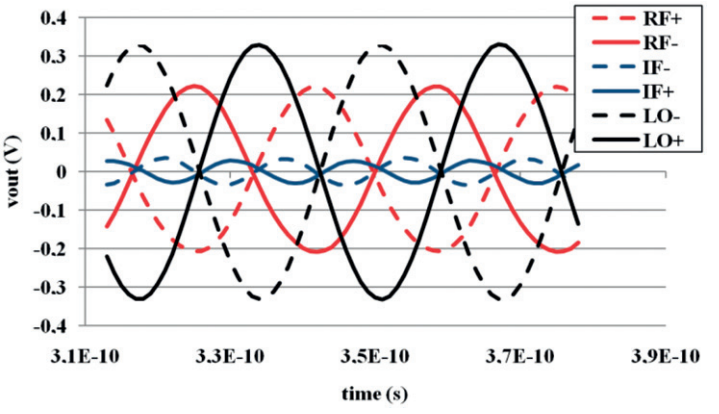

Figure 6. 60 GHz doubler transient simulation results.

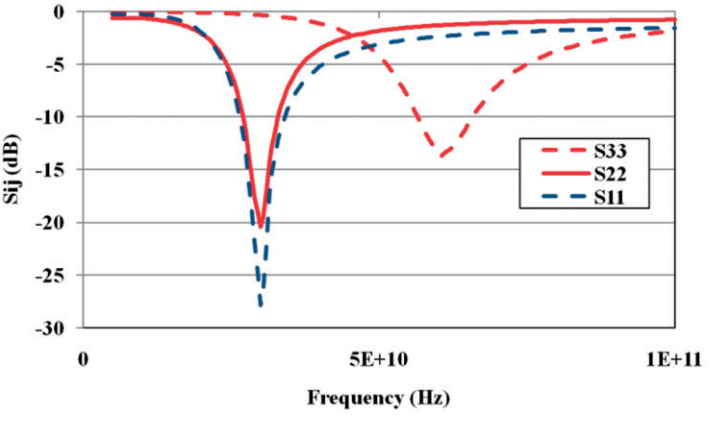

Figure 7. 60 GHz doubler input/output matching.

quadrature output the relationship between resistance R, capacitance C and frequency ω is given by Behbahani et al. (2001) and Tillman and Sjoland (2001),

$$R \cdot \omega = 1 \tag{2}$$

The values of R and C should be chosen according to Equation (2) and the frequency value. For the design that is described here $f = 30$ GHz, $\omega = 2 \cdot \pi \cdot f$, $R = 48$ Ohm and $C = 112$ fF.

This passive polyphase filter can be altered into an active one, if the resistors of Figure 8 are replaced by transconductors (Tillman and Sjoland 2001). Such an active polyphase filter is presented in Figure 11. This topology behaves in the same way as the passive one, if g_m equals $1/R$. As it is presented in Figure 11, the resistors are replaced by CMOS inverters. The advantage of this active topology is that the inverters' supply voltage can be adjusted externally in order to compensate against phase shifts different than 90°.

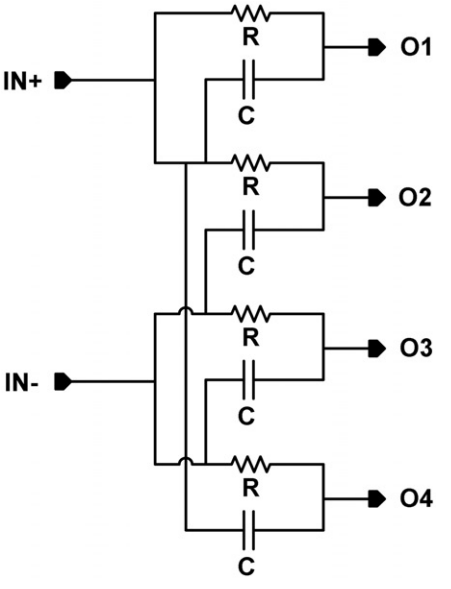

Figure 8. Passive polyphase pilter.

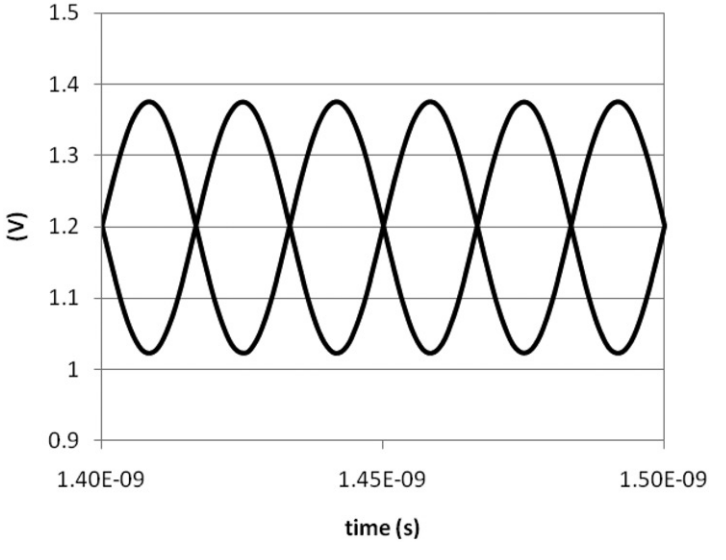

Figure 9. Input signals of the polyphase filter.

Changing the supply voltage *Vctrl* of the polyphase filter, the g_m of the inverters is also changed resulting to a variable time constant, which consequently gives a different phase.

The active polyphase filter consists of two stages, which can ensure larger bandwidth in comparison with one stage. Stage 1, as presented in Figure 11, generates a quadrature signal and Stage 2 reduces the quadrature error and makes the filter broadband.

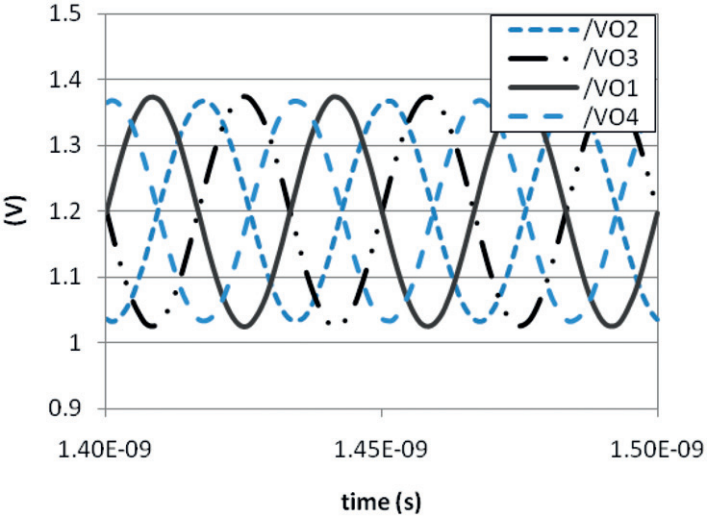

Figure 10. Output signals of the passive polyphase filter.

The resistor R has value equal to 9.6 KΩ, the capacitors C_1–C_3 have values 215.63 fF and C_4 is 36.98 fF. The PMOS transistors have dimensions 32.04 μm/100 nm and the NMOS transistors 16.02 μm/100 nm.

The outputs of the active polyphase filter are depicted in Figure 12. The results of the active polyphase filter in Figure 12 are measured for *Vctrl* voltage equal to 1.2 V. The values of the phase versus *Vctrl* is shown in Figure 13. The phase noise of the active polyphase is −156 dBc/Hz at 1 MHz. Post-layout simulation results showed a maximum amplitude unbalance of ±0.7 dB whereas the maximum phase mismatch from 90° is less than ±1.5° in the 27 GHz to 33 GHz frequency range.

2.4. *LO amplifiers*

As explained above, the output signal of the doublers is significantly attenuated and is not able to drive the next stages due to the fact that the input transistors are characterised by large capacitive load. Therefore, amplifiers are required to be inserted to amplify sufficiently the signals from the doublers to the next stage. The amplification in intermediate stages is important because otherwise if the signal becomes too low, the next stages may not operate at all. For this purpose, local oscillation (LO) amplifiers at 30 GHz and 60 GHz are employed. The schematic of the amplifiers is shown in Figure 14. The first LO amplifier gives a peak gain 7.3 dB at 30 GHz with a bias current 15 mA, as shown in Figure 15. The plot diagram of the phase noise is shown in Figure 16 and is found below −155 dBc/Hz at 1 MHz. The second amplifier gives a peak gain at 60 GHz with a bias current 25 mA (Figure 17). The phase noise (Figure 18) is again below −155 dBc/Hz at 1 MHz. Both amplifiers are based in the topology shown in Figure 14, with suitable modifications in order to fit to the operation frequency and the bias current. In this way, the transistor sizes match with the bias current of 15 mA and 25 mA respectively, while the

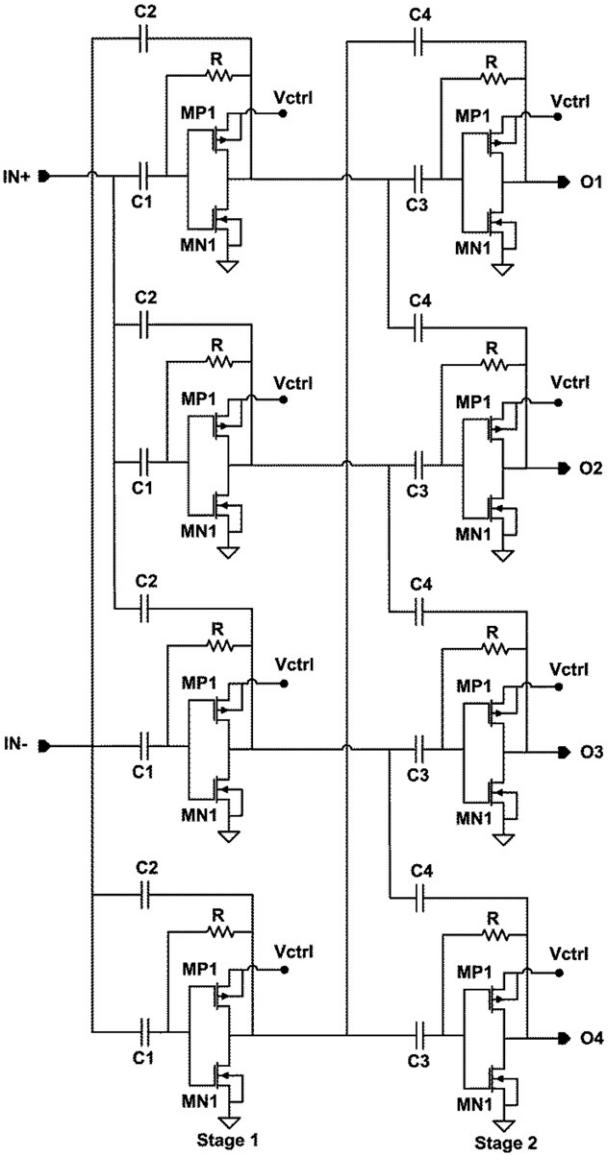

Figure 11. Active polyphase filter.

inductor value is chosen for operation frequency at 30 GHz and at 60 GHz. The value of each element of the LO amplifiers is depicted in Table 3.

3. Simulation results

The layout of the frequency quadrupler has been designed using IBM 9RF process. The final layout is shown in Figure 19. The total area is 2 mm × 0.7 mm, which is relatively

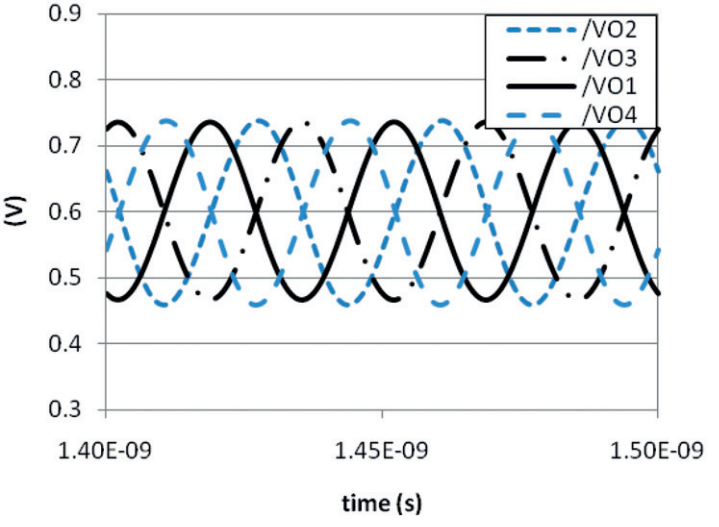

Figure 12. Output signals of the active polyphase filter.

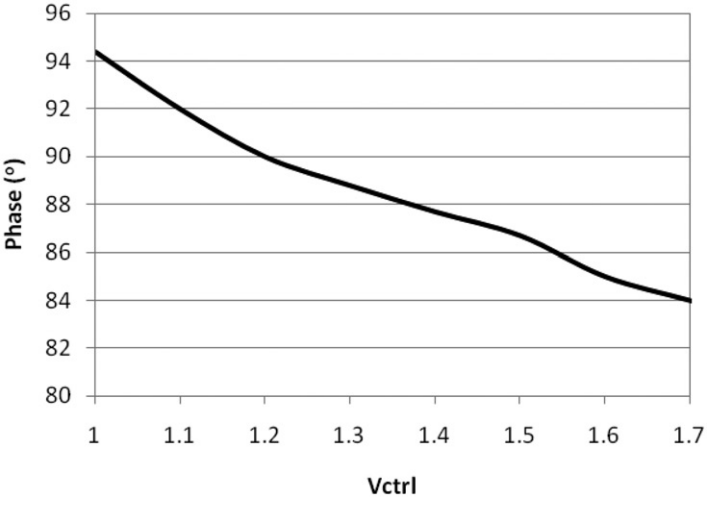

Figure 13. Phase shift control.

large due to the fact that we followed the design rule which suggests that a relatively large distance exists between the spiral inductors and the framed substrate/bulk connections. This rule was strictly kept in order to minimise any side effect in the circuit operation. Had this rule been relaxed either because the specific process permits it or by our decision, then the total area would be significantly reduced. Regarding interconnections, the process offers enhanced electromagnetic models for coplanar waveguides and coupled coplanar waveguides which have been used in the design. The supply voltage is 1.2 V and the total power dissipation, including supporting circuits, like the bias current generators,

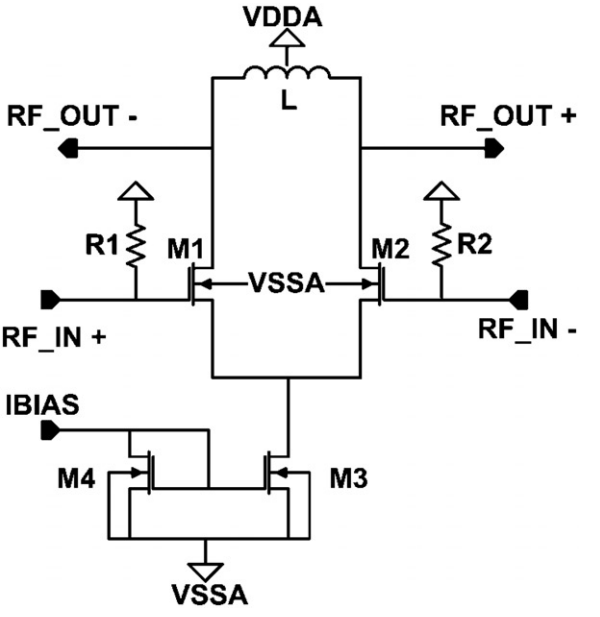

Figure 14. The schematic of the LO amplifier.

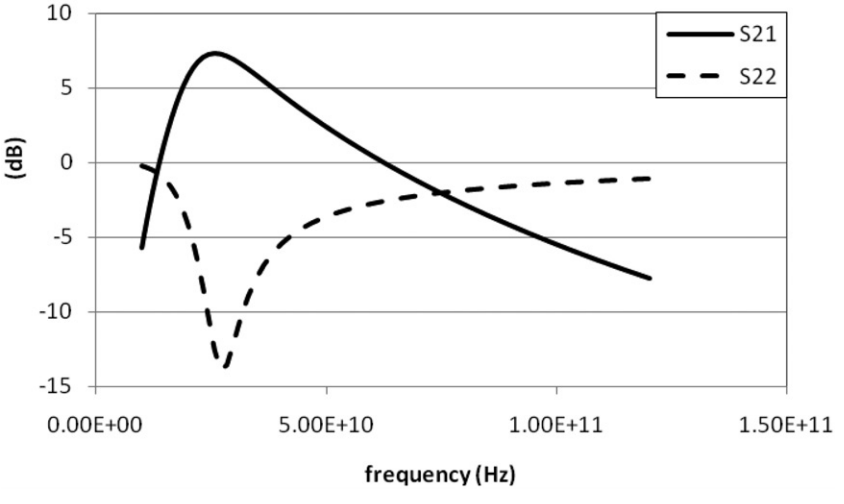

Figure 15. Simulation results of the LO amplifier at 30 GHz.

is 120 mW. Each LO amplifier at 30 GHz dissipates 18 mW and each LO amplifier at 60 GHz dissipates 30 mW. The 60 GHz output after post-layout simulations is depicted in Figure 20.

The effective rejection of unwanted harmonics is higher than 43 dB for the second harmonic and more than 56 dB for the third one respectively. The total harmonic distortion (THD) is about 1%. A maximum output power of −8.2 dBm in a bandwidth of

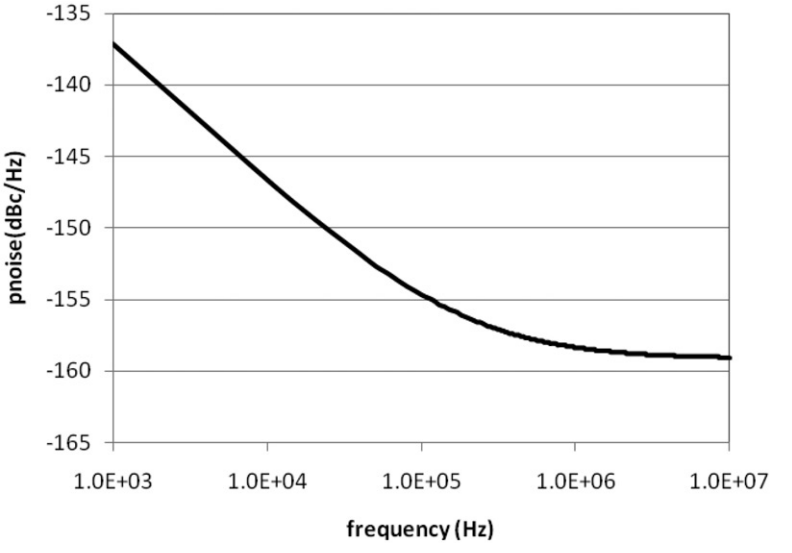

Figure 16. Phase noise simulation results of the LO amplifier at 30 GHz.

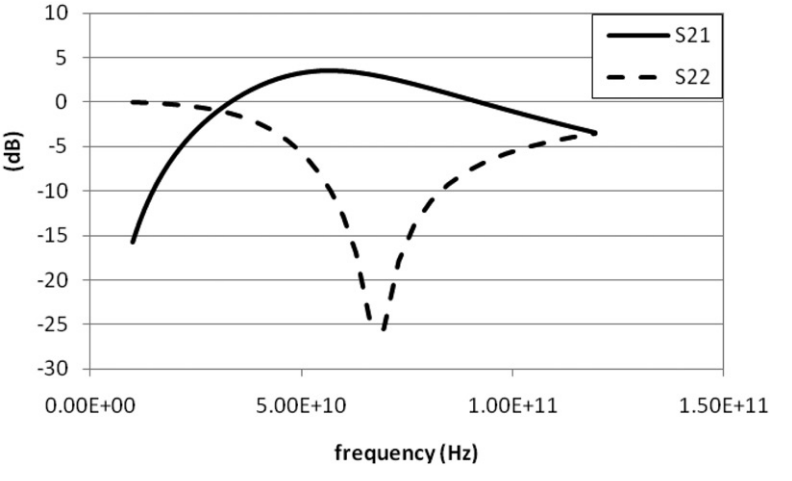

Figure 17. Simulation results of the LO amplifier at 60 GHz.

9.5 GHz was obtained, where the bandwidth of the quadrupler is defined as the frequency range over which the conversion loss remains within 3 dB of the maximum value. The phase-noise degradation given by $20 \cdot \log(N)$, where N is the multiplication order, is known to be the minimum degradation in an ideal frequency multiplier. In the case of a quadrupler, the theoretical value is 12 dB, whereas the proposed scheme degrades the phase noise by approximately 14 dB. The performance summary is presented in Table 4.

A comparison with other designs in literature is summarised in Table 5. As it can be deduced by this table, the implementations in non-CMOS technologies may offer higher

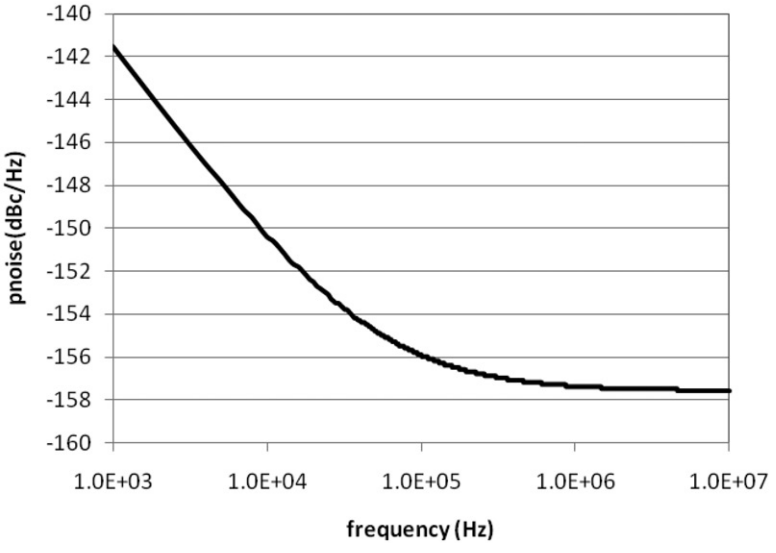

Figure 18. Phase noise simulation results of the LO amplifier at 30 GHz.

Table 3. LO amplifiers.

Element	Value (30 GHz LO Amp)	Value (60 GHz LO Amp)
M1, M2	52 μm/100 nm	52 μm/100 nm
M3	160 μm/400 nm	280 μm/400 nm
M4	16 μm/400 nm	16 μm/400 nm
R1, R2	2.8 K	2.8 K
L	373 pH	116 pH

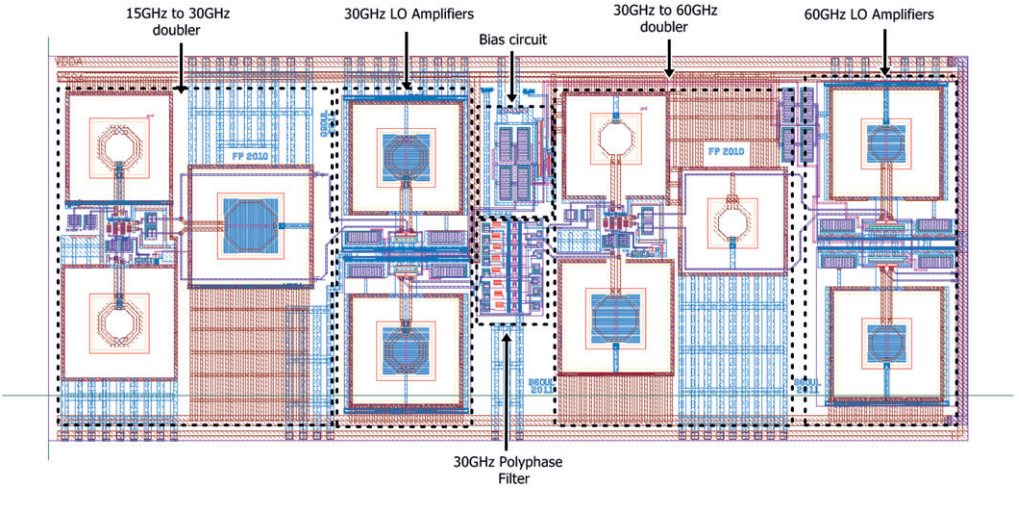

Figure 19. The layout of the frequency quadrupler.

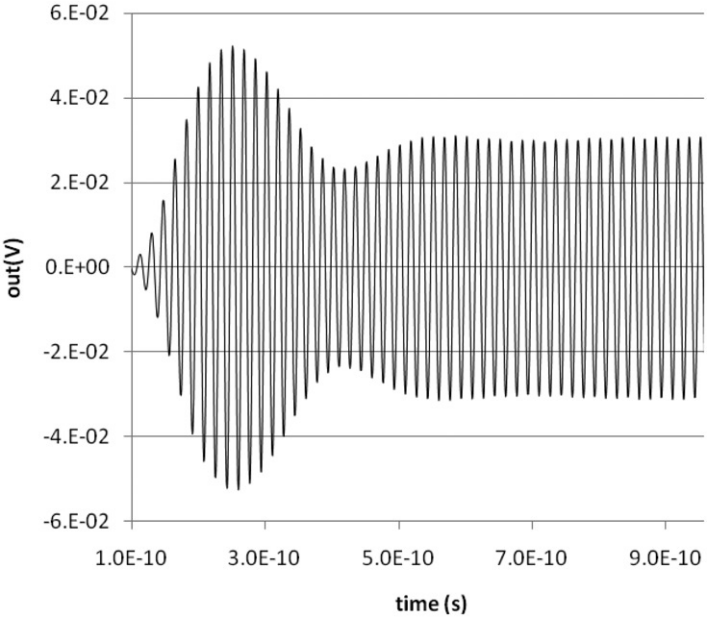

Figure 20. The 60 GHz output of the frequency quadrupler.

Table 4. Performance summary.

Quantity	Experimental data
Process	IBM 90-nm CMOS
Devices	MOSFET 1.2 V, $V_{TN} = 0.42$ V
Nominal supply voltage	1.2 V
Conversion loss	9.3 dB
3 dB bandwidth	9.5 GHz
Output swing	70 mV
Output load	50 Ω
Power dissipation	120 mW
Area	1.4 mm^2

output power, higher gain and lower conversion loss, in the cost though of increased area and power consumption along with the expensive manufacturing cost. If compared with the CMOS implementations reported, this work offers better harmonics rejection, higher bandwidth, comparable output to input ratio (Kantanen et al. 2008). The power consumption and die area are well within the limits set by previously reported works when taking into account the x4 factor and the differential implementation. In conclusion, the more gain and performance is required the more power and area should be consumed.

4. Conclusion

A quadrupler topology from 15 GHz to 60 GHz designed in a CMOS 90 nm technology is presented in this article. The basic blocks were two double balanced passive mixers and an

Table 5. Performance comparison.

Ref	Technology	Type	Pout/Pin dBm	Fout GHz	BW %	Reject. dB	Pdc mW	Area $(mm)^2$
Karnfelt et al. (2006)	0.15 μm pHEMT	sing. x8	8/0	60 GHz	16.6	28	450	8
Kim et al. (2008)	0.15 μm GaAs pHEMT	sing. x2	18/3	60 GHz	8.3	25	N/A	3.72
Schefer (2002)	0.1 μm InP HEMTs	sing. x4	0/6	60 GHz	8.3	20	90	0.79
Ito et al. (2006)	0.15 μm AlGaAs/InGaAs	sing. x12	0/−5	60 GHz	8.3	20	295	2.88
Liu et al (2010)	0.8 μm SiGe HBT	sing. x2	−1.6/0	60 GHz	30	13	N/A	N/A
Hara et al. (2009)	65 nm CMOS	inj. x4	−75/9	60 GHz	11.6	N/A	6.8	0.018
Kantanen et al. (2009)	90 nm CMOS	sing. x2	−4.2/5	60 GHz	11.6	10.8	13.7	0.7
Chan and Long (2008)	90 nm CMOS	inj. x3	−24.7/0	60 GHz	15	N/A	23.8	0.09
This Work	90 nm CMOS	bal. x4	−8.2/1.1	60 GHz	15.8	40	120	1.4

inj: injection locked, sing: single-ended, bal: balanced

active polyphase filter with some LO amplifiers. The supply voltage was 1.2 V and the total power dissipation including all the supporting circuits was 120 mW. Post-layout simulation results are presented to verify the topology operation. Compared with designs available in the literature the proposed quadrupler offers differential inputs and outputs, better harmonics rejection, higher bandwidth, comparable output to input ratio, less power consumption and die area.

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