

# A 0.5 - 5.5 GHz Distributed Low Noise Amplifier

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## ABSTRACT

The Low Noise Amplifier (LNA) presented in this work is a 3-stage fully integrated Distributed Amplifier (DA) using a 0.35  $\mu\text{m}$  BiCMOS SiGe process. The circuit was designed for integration and for this reason the different parasitical phenomena that concern the spiral inductors and the packaging were evaluated in detail. Noise Figure (NF) and linearity were also investigated through simulations. The designed amplifier offers a gain of about 7 dB with a gain flatness of  $\pm 0.6$  dB over the bandwidth 0.5-5.5 GHz and an average noise figure of 3.2 dB. The RF input port is matched to 50  $\Omega$ , with worst-case return loss of -10 dB over the whole bandwidth. The input-referred  $P_1$  dB point varies from 2.2 dBm at 1 GHz to 3.1 dBm at 5 GHz. Within the same bandwidth the IP3 varies from 6 dBm to 13.3 dBm. The estimated power consumption is 82.5 mW from a 3V power supply.

**Keywords:** Distributed Amplifier, Inductor Model, Noise Figure

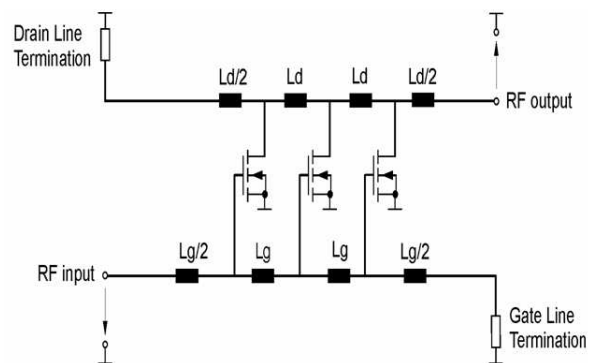
## 1. INTRODUCTION

Distributed amplification is a concept which can be traced back to 1936 [1]. The distributed amplifier [2, 3, 4] has the advantage of maintaining an almost flat gain curve over a broad region of frequencies. Due to that, it can be used as a LNA for present and future applications in multi-band receivers (GSM-Quadband, W-CDMA, and WLAN). The design approach for a DA uses the special characteristics of the transmission lines and achieves a new trade-off between gain and delay instead of the usual maximum gain-bandwidth product of other conventional amplifiers. Theoretically by using properly designed transmission lines we can obtain infinite bandwidth without any gain restriction for the amplifier. The only penalty is the insertion of delay for the signal that travels towards the output. In a real design, where attenuation and loss factors are inevitable, the theoretically infinite bandwidth no longer holds true. Additionally, the distributed nature of the amplifier and the loss mechanisms impose painful compromises

between important design parameters such as gain, noise figure, bandwidth, power consumption, and linearity. For these reasons it is very challenging to design and implement integrated distributed amplifiers that can satisfy wideband operation specifications with reasonable power consumption. The need for multiband operation in modern receiver architectures demands the fulfilment of multiple requirements. The receiver must operate in several frequency bands with variable bandwidths. In addition linearity and noise requirements vary, depending on the modulation scheme and the target application. In this paper we design and investigate a 3-stage DA taking into account transmission line losses and inductor and packaging parasitics. The result is an LNA with the desired flat gain response and linear transmission phase, such that it meets the multi-band (or wide-band) receiver specifications. The design methodology of the proposed amplifier is given in Section 2, whereas in Section 3 simulation results are described. Finally the conclusion is given in Section 4.

## 2. AMPLIFIER DESIGN

The inherent gate and drain impedances of the transistors are matched with lumped inductors to create artificial transmission lines for both the input (gate line) and the output (drain line) as shown in Fig. 1. These lines are coupled by the transconductances of the transistors.



**Fig. 1:** Basic Distributed Amplifier Topology

The RF signal from the antenna which is transmitted through the gate line, triggers the cascaded transistor stages producing output signals at each stage which pass through the drain line to the output port. The characteristic impedance of the designed trans-

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mission lines is  $50 \Omega$ . Furthermore as shown in Fig. 1 appropriate resistive terminations should be used to avoid reflections in both signal paths. Since the propagation delay of the formed transmission lines is the same, the output signals will be added coherently. This property allows the circuit to operate as an amplifier at frequencies where the single transistor stages provide no longer voltage amplification. Transmission lines -which theoretically achieve, a frequency independent trade-off between gain and bandwidth- are formed by incorporating the parasitic transistor capacitances into the circuit topology and using lumped inductors between the amplification stages. The drawback is the increased propagation delay for the signal travelling towards the output port. Thus, for applications where the resulting delay is acceptable the DA is an alternative solution for multi-band operation instead of using other approaches with parallel receiver paths which lead to increasing chip area and costs.

## 2.1 Ideal DA

The design procedure is based on a model described in other works [3, 4, and 5]. In order to obtain a realistic behaviour of the designed circuit several design steps are required. Initially, the DA was designed using ideal circuit elements and interconnections. The next design step introduced microstrip line segments which replace the ideal metal interconnections between the circuit components. Finally parasitics of the spiral inductors and packaging terminations were taken into account and equivalent models were used in the circuit simulator. For the calculation of the main parameters of this circuit we used the methodology proposed by Ballweber et al. [4]. The staggering technique is chosen to provide a flat response in the operating bandwidth 0.5 - 5 GHz. Staggering leads to a lower cutoff frequency for the drain line than for the gate line. By accepting this technique and assuming image-matched terminations for both lines, the voltage gain can be written [4] as:

$$A \cong \frac{-gm}{2\sqrt{1 - (\omega/\omega_{cg})^2}} \sqrt{\frac{L_d}{C_d}} \cdot \frac{\sinh \left[ \frac{N(\gamma_g - \gamma_d)}{2} \right]}{\sinh \frac{(\gamma_g - \gamma_d)}{2}} e^{-N(\gamma_g + \gamma_d)/2} \quad (1)$$

where  $N$  is the number of stages,  $g_m$  is the stage transconductance,  $\gamma_g$  and  $\gamma_d$  are the propagation constants of the gate and the drain lines respectively and  $\omega_{cg}$  is the cutoff frequency of the gate line.

At the termination ports we used  $m$ -derived half sections as shown in Fig. 2. These filter sections achieve an impedance matching to resistor terminations over a broad frequency region as described in [8]. Thus they are well suited for our amplifier design in order to achieve the desired flat gain characteristic.

$L$  and  $C$  are the filter-section components,  $m$  is the half-section constant and  $Z_0$  the resistive termination

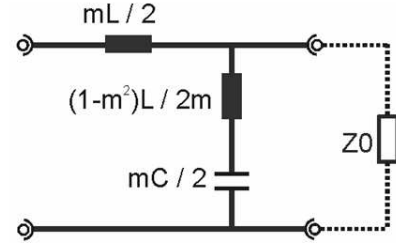


Fig.2:  $m$ -derived half section

of the line. As already mentioned this value is chosen to be  $50 \Omega$  in order to match the antenna feed point impedance at the input port of the amplifier stage.

## 2.2 Inductor & Parasitic Model - Final DA

The next design step was to replace the ideal metal connections between the different circuit elements with microstrip line segments. The added components insert a more realistic behaviour for those conducting connections. These microstrip components are described fully by their length, width and substrate model. For estimating the width of each connection we used the current density of the metal layer that is used for implementing the connections (e.g. top-metal layer) and the corresponding current value for each circuit branch. The microstrip segment lengths were estimated by a basic layout approach and the substrate model was generated appropriately using the  $0.35 \mu m$  technology process parameters.

The final step of the procedure is the insertion of equivalent models for the parasitics concerning the spiral inductors and the package terminations. Planar spiral inductors can be implemented in different ways. One possibility is the square form shown in Fig. 3 using two different metal layers. In order to determine the geometry pattern of the needed inductor values we used Ansoft HFSS.

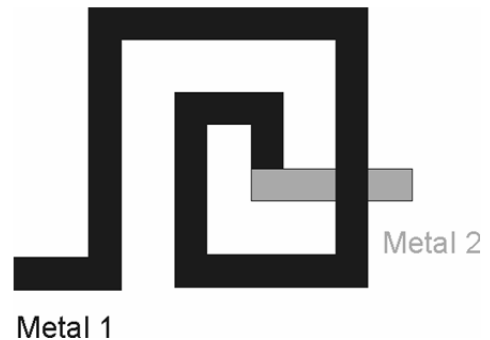


Fig.3: Spiral Inductor

Figure 4 illustrates the equivalent model of a spiral inductor which is a  $\Pi$ -network. The series elements  $L_s$  and  $R_s$  represent the actual spiral inductance and resistance respectively, while the shunt element  $C_p$

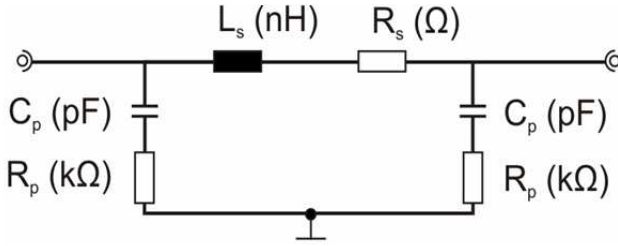


Fig. 4: Spiral Inductor Model

is the parasitic capacitance to the substrate and  $R_p$  the resulting substrate resistance. Both series elements are in generally frequency dependent because of the induced eddy currents in the substrate and the skin effect. The high substrate resistivity of 19  $\Omega\text{cm}$ , combined with the inductor implementation on the top-metal layer, suppresses the influence of eddy currents on the inductance value. Furthermore, calculations showed that the corresponding skin depth at the highest frequency of interest (e.g. 5.5 GHz) results in negligible change of the total spiral resistance, thus we can consider it frequency independent. Therefore, the model parameters could be calculated in a straightforward manner from the geometry of the spiral inductor and the process parameters using equations (2a-2c).

$$R_s = R_{sh} \frac{l}{w} \quad (2)$$

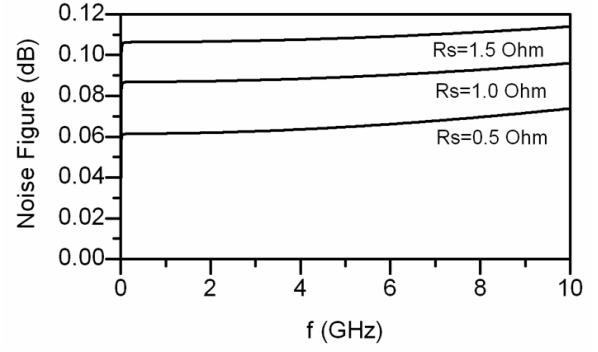
$$C_p = \epsilon_0 \cdot \epsilon_r \frac{w}{h_{Si}} \quad (3)$$

$$R_p = \rho_{Si} \frac{l}{w \cdot h_{Si}} \quad (4)$$

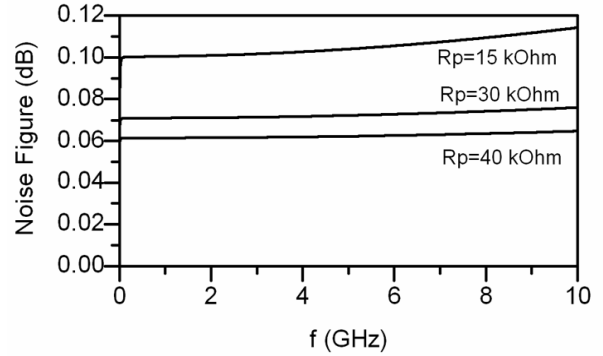
Where  $l$  and  $w$  are the spiral length and width, while  $h_{Si}$ ,  $\rho_{Si}$  and  $\epsilon_r$  are the height, resistivity and relative permittivity of the substrate respectively. Finally  $\epsilon_0$  is the dielectric constant of the vacuum.

Figure 5 shows the noise level added by the inductor model used in the simulation. Two parametric simulations are presented where the resistive elements  $R_s$  and  $R_p$  were used as sweep parameters. Typical values for the other model parameters were used in the simulations. The diagrams show that the additive noise level increases with raising series resistance  $R_s$  (Fig. 5.a) and decreases with increasing substrate resistance  $R_p$  (Fig. 5.b). An ideal implementation would result in spiral inductors with low metal and high substrate resistance respectively. Unfortunately, these elements are geometry- and technology- dependent as can be seen from Eqs. 2a-2c. Thus, a compromising solution is desirable, which could be implemented in the selected technology process. Generally, using integrated passive elements featuring low quality factors will degrade further the overall circuit performance, as will be shown in the following section.

The final amplifier design, which includes the detailed models for the spiral inductors and packaging,



5.a) Noise Figure for  $R_s$  sweep



5.b) Noise Figure for  $R_p$

Fig. 5: Noise Figure of the Inductor Model

is shown in Fig. 6. Instead of the ideal spiral inductors we used in the final design the equivalent 3-port model of Fig. 4. The small values of the metal resistance that were calculated for the inductor models result in unnoticeable changes at the bias level of the circuit branches. Thus, the bias state of the transistor stages is not influenced. One consequence due to the package model is that we can ignore two of the initially used inductors and replace them with the already existing package inductances of the model.

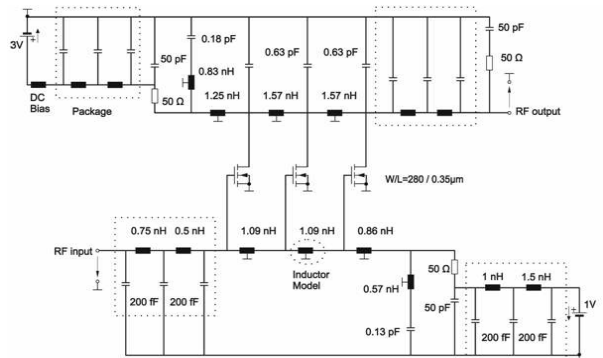


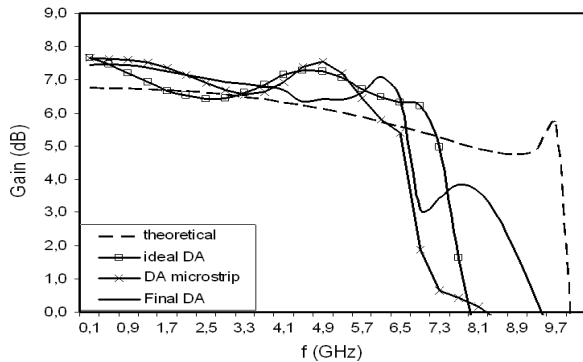
Fig. 6: Distributed Amplifier with Parasitics

The noise figure of the low noise amplifier has a significant impact on the overall receiver performance. Therefore it is important to minimize the noise level from the LNA itself. For calculating the noise level we used the theory introduced by Aitchin-

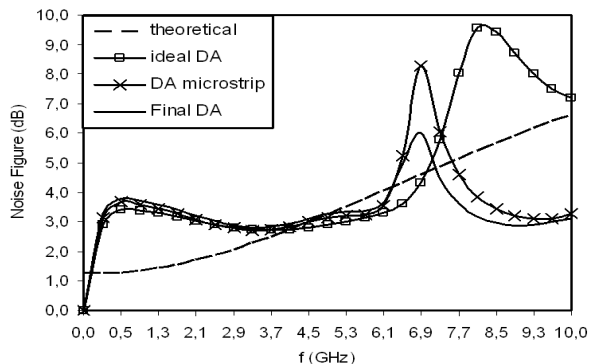
son [6] concerning the intrinsic noise sources of FET transistors for distributed amplifiers.

### 3. RESULTS

The gain and noise figure curves for the theoretical calculations, the ideal DA, the design with the microstrip lines (DA microstrip) and the final design (Final DA) are presented in Fig. 7 and 8 respectively. The theoretical gain curve was calculated according to Beyer *et. al* [5].



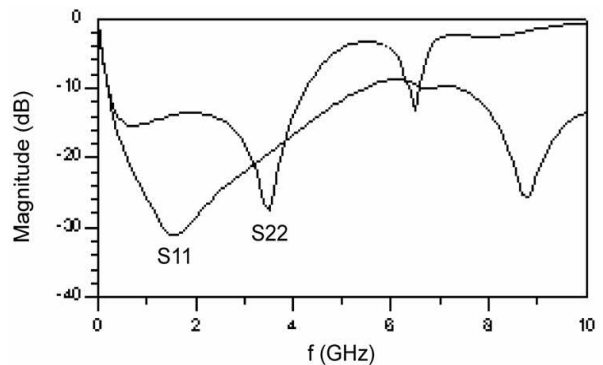
**Fig.7:** Gain Curves of the Design Stages



**Fig.8:** Noise Figure of the Design Stages

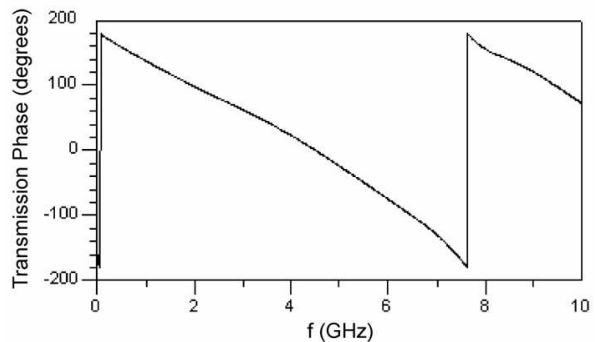
The final design, including microstrip line segments and parasitics, offers smaller gain than the foregoing ones but maintains the best flatness over the bandwidth 0.5 - 5.5 GHz. All designs lead to a smaller cutoff frequency in comparison to the ideal DA which treats the circuit components, mainly inductors, as ideal and thus ignores effects like self-resonance frequency. The difference between theoretical and simulation curves for the noise figure, shown in Fig. 8, results from the fact that the method used for calculating the noise figure of the DA concerns only the intrinsic noise sources of the FETs. The noise contributed by the conducting connections and spiral inductors is not included in this theory. We also observe that the final DA has the highest noise figure across the operating bandwidth. This is due to the noise added by the inductors and the conducting connections represented by the microstrip elements.

However, the noise figure remains below 4 dB across the 0.5 - 5 GHz frequency range. Finally, the input and output port matching parameters of the proposed amplifier are plotted in Fig. 9. We must emphasize that by adding parasitics the total response of the circuit is degrading. The highest degradation concerns output port matching that turns out to be poor for frequencies above 4 GHz. To avoid such undesired behavior the designer could optimize the circuit parameters and use more convenient package terminations.



**Fig.9:**  $S_{11}$  and  $S_{22}$  Parameters of the final DA

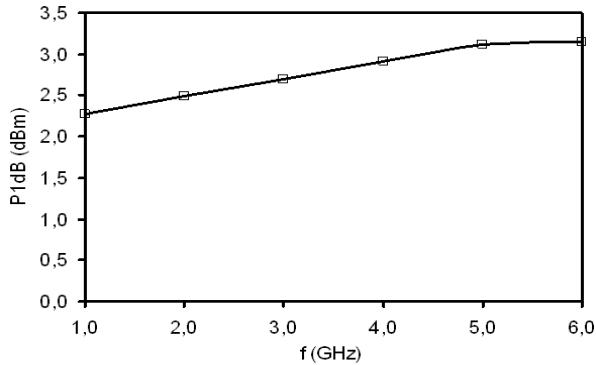
Except for the gain and noise figure, linearity (in magnitude and phase) is also an important characteristic of a low noise amplifier. As shown in Fig. 10 the transmission phase curve is quite linear in the operating bandwidth 0.5-5.5 GHz. This indicates an almost constant propagation delay for the traveling signal. Such a response is highly desirable in broadband operation since signals with rich harmonic index will not suffer dispersion by passing through the amplifier stage. All harmonic frequencies will propagate with an almost constant delay through the circuit. This linear phase curve is a consequence of the used topology and underlines once more the excellent broadband properties of the distributed amplifier.



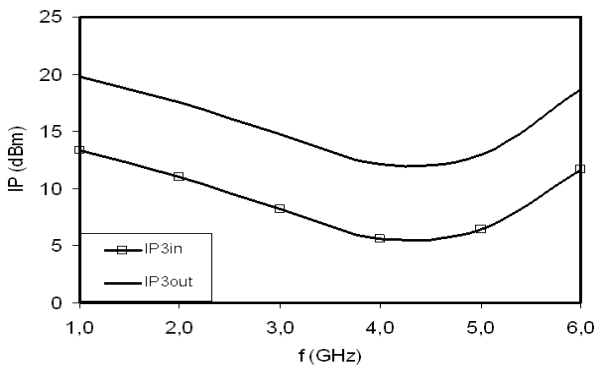
**Fig.10:** Transmission Phase Curve of the DA

Linearity performance is also determined by the 1-dB compression point (P1dB) shown in Fig. 11 and the third-order intercept point (IP3) shown in

Fig. 12. Both curves were obtained by simulations indicating the linearity performance of the system. The power level of the two input tones used in IP3 simulations is chosen to be -20dBm. All simulation results presented in this work, linear and nonlinear, have been obtained by using Agilent's ADS simulation tools.



**Fig.11:** 1 dB Compression Point of the final DA



**Fig.12:** Third Order Intercept Point of the final DA

In Table 1, we attempt a comparison with previously reported research in integrated distributed amplifiers.

**Table 1:** Design Performance

Design	Gain (dB)	Bandwidth (GHz)	NF (dB)	Power (mW)
Sullivan <i>et. al</i> [3]	5.0±1.2	0.3-3	5.10	54
Ballweber <i>et. al</i> [4]	6.5±1.2	0.5-4	6.86	83.4
Ker <i>et. al</i> [7]	4.9±1.1	1.0-9.0	5.3	-
this work (Final DA)	6.9±0.6	0.5-5.5	3.24	82.5

The tabulated values of the gain and noise figure correspond to mean values within the operating bandwidth. The performance obtained by the final design is very promising in terms of gain flatness, bandwidth

and noise level. Furthermore, the proposed approach operates at comparable power consumption levels. Performance degradation regarding mainly the noise figure and the gain flatness is expected when the system is implemented in integrated form and verified by measurements.

#### 4. CONCLUSIONS

In this paper, a complete design of a distributed low noise amplifier that achieves a 5 GHz bandwidth is demonstrated. Identifying loss mechanisms and predicting the integrated inductor performance are key goals for the circuit characterization. The design of distributed amplifiers involves a large number of trade-offs that are partially conflicting and make their implementation in integrated circuit a challenging task. The main design goals focus on the gain, noise figure, bandwidth, power consumption, linearity and matching of the input and output ports. The mechanisms that introduce difficulties in satisfying the design goals for DA are the integrated nature of the circuits and the non-ideal behavior of their components such as inductors and package elements. In this paper we have successfully designed for implementation a 3-stage DA with a gain of about 7 dB, gain flatness of  $\pm 0.6$  dB over the bandwidth of 5 GHz and an average noise figure of 3.2 dB. The amplifier has satisfactory linearity and is estimated to dissipate 82.5 mW from a 3 V power supply.

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