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A study of superharmonic injection locking in multiband frequency dividers

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ABSTRACT

A superharmonic voltage-controlled injection-locked frequency divider, implemented using a modified Colpitts oscillator operating at 2.5, 5 and 10 GHz and a cross-coupled LC oscillator operating at 1.25, 2.5 and 5 GHz, is demonstrated. The proposed triple-band operation is achieved by employing a novel technique that uses pin-diodes and negative power supply. The discrete dividers, built with low noise hetero-junction FETs and high-frequency SiGe BJTs, are described theoretically while their functionality is proven experimentally. Additionally, a short phase noise analysis, which is missing in the literature, is given. Phase noise, frequency range of operation, and locking range measurement results are presented. Finally, post-layout simulation results of a 5 GHz fully differential injection-locked frequency divider, implemented in a 0.25 μm SiGe process are provided. Copyright © 2010 John Wiley & Sons, Ltd.

KEYWORDS
injection-locking; phase noise; frequency divider

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1. INTRODUCTION

Frequency dividers are widely used in a variety of communication systems including carrier recovery and phase locked loops. Although digital frequency dividers offer wide bandwidth, they suffer from large power consumption. On the other hand, as the high-frequency operation performance of the analog dividers is better they are used in high-frequency demanding applications while offering low power consumption. However, they exhibit limited bandwidth and it is difficult to offer division ratios greater than two. A well-suited solution is the voltage-controlled injection-locked frequency divider (VCILFD), which provides extended bandwidth and, a broad range of division ratios. The drawback of the above-mentioned method is that conventional VCILFDs (apart from the use of ring oscillators) require either an LC or a short-stub resonator, which results in a large chip area.

During the injection locking process, a local oscillation can be locked to the frequency and phase of external injection signal under proper conditions. After locking the frequencies of the local oscillation (ω_{osc}) and the external signal (ω_{inj}) are equal ($\omega_{osc} = \omega_{inj}$) while the phase difference between them is kept constant. The injection-locking/coupling technique is used for phase noise reduction [1], frequency division [2, 3], or multiphase and hyperchaos generation [4–7]. The phenomenon is unwanted when injection through substrate or other environmental coupling results in an unintended lock.

Furthermore, an oscillator can be locked to a signal whose frequency equals to a harmonic of the oscillation frequency (superharmonic injection) or to a subharmonic of the oscillation frequency (subharmonic injection). The phase noise performance of sub- or superharmonic injection-locked oscillators is also better compared with free-running ones.

Consequently, subharmonic injection can be used for frequency multiplication (the output frequency of the injection-locked oscillator is a harmonic of the injected frequency), whereas superharmonic injection can be used for frequency division (the output frequency of the injection-locked oscillator is a subharmonic of the injected frequency).

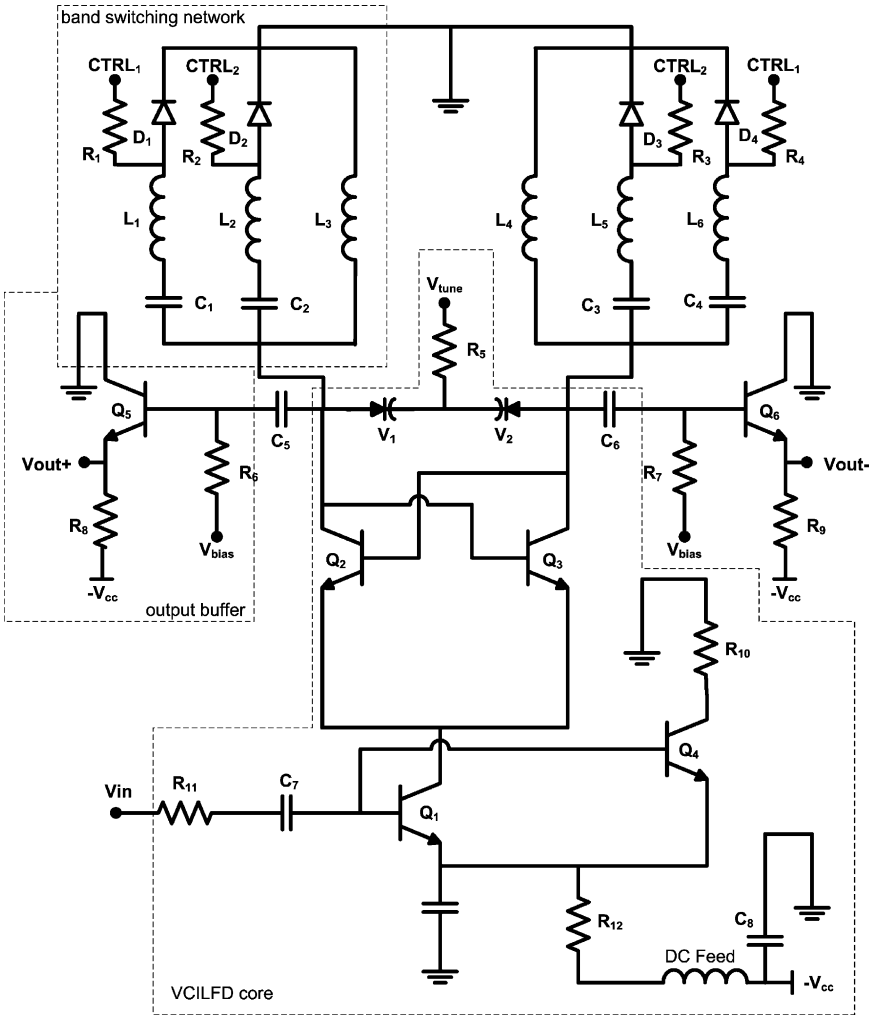

Figure 1. Circuit topology of the single-ended input differential output VCILFD.

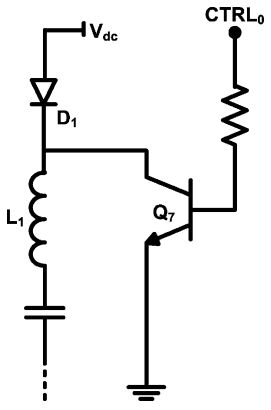

Figure 2. Alternative frequency band switching.

Several methods are proposed for injection-locked frequency division operating at gigahertz frequencies [8–14]. In this work, we present multiband design solutions for frequency division by employing injection locking. In order to achieve multiband operation, a network including inductors and pin diodes for the microwave switch control circuit has been incorporated. Furthermore, due to high input sensitivity, we can achieve locking up to the 8th harmonic of the free-running frequency with both the topologies, resulting in division ratios of 2, 4 and 8. The post-layout simulation results of a 5 GHz fully differential (differential-input, differential-output) VCILFD implemented in a 0.25 μm SiGe process are reported. Finally, we introduce a short analysis, missing in the literature, which can be used to predict the phase noise performance of the VCILFD, given that the PSD of the phase noise of the input signal and the PSD of the internal phase noise are known.

2. DESIGN

2.1. Circuit description

A VCILFD is usually implemented using a Voltage-Controlled Oscillator (VCO) in which an additional

Table I. Frequency range performance and division ratios.

Input frequency band	:2 (GHz)	:4	:8
10	4.482–5.418	1.854–2.80 GHz	1.063–1.397 GHz
5	1.891–2.759	1.156–1.30 GHz	x
2.5	1.185–1.285	x	x

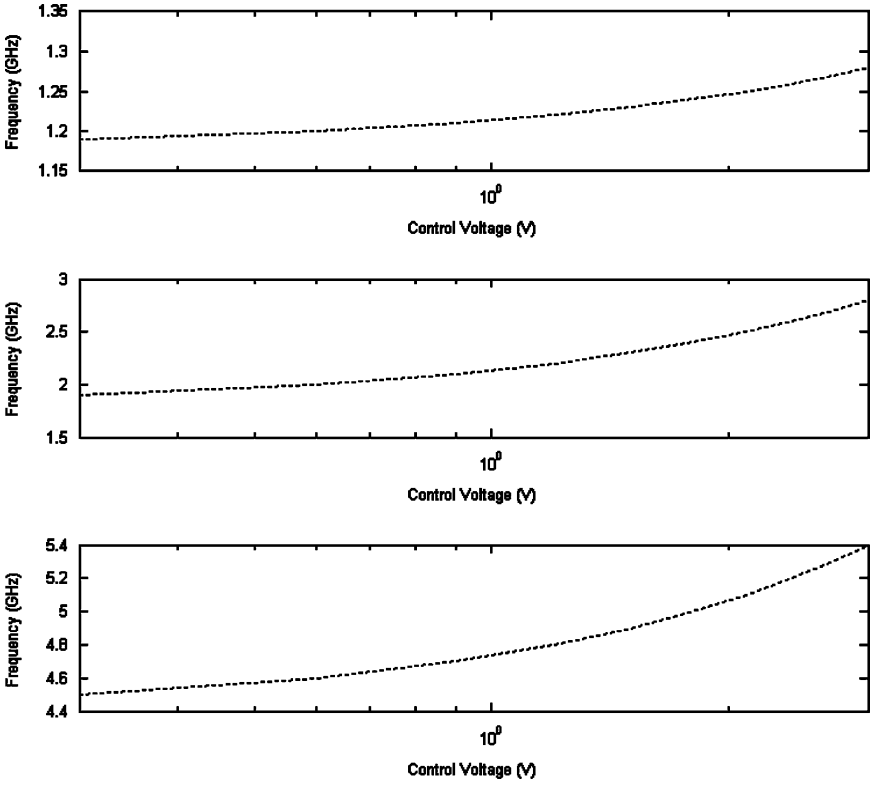

Figure 3. Simulated tuning range at the three different frequency bands.

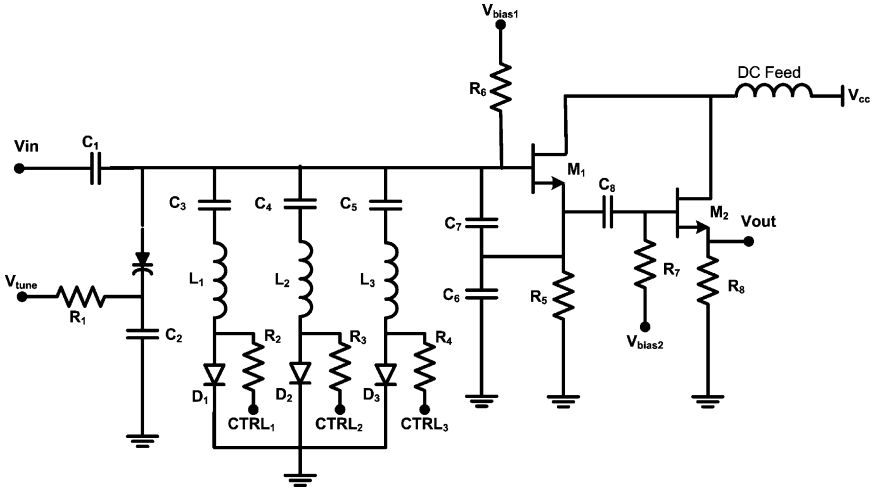

Figure 4. Schematic of the single-ended input single-ended output VCILFD.

Table II. Frequency range performance and division ratios.

Input frequency band	:2 (GHz)	:4	:8
20	8.875–11.525	4.425–5.475 GHz	1.713–2.987 GHz
10	4.488–5.412	1.863–2.837 GHz	x
5	1.894–2.806	x	x

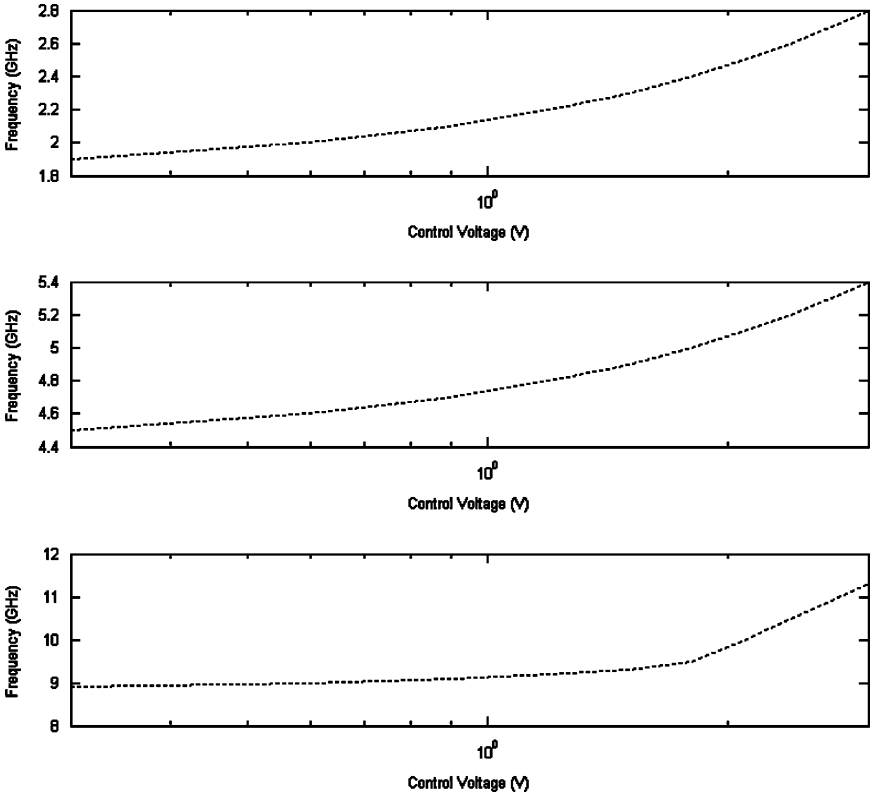

Figure 5. Simulated tuning range at the three different frequency bands.

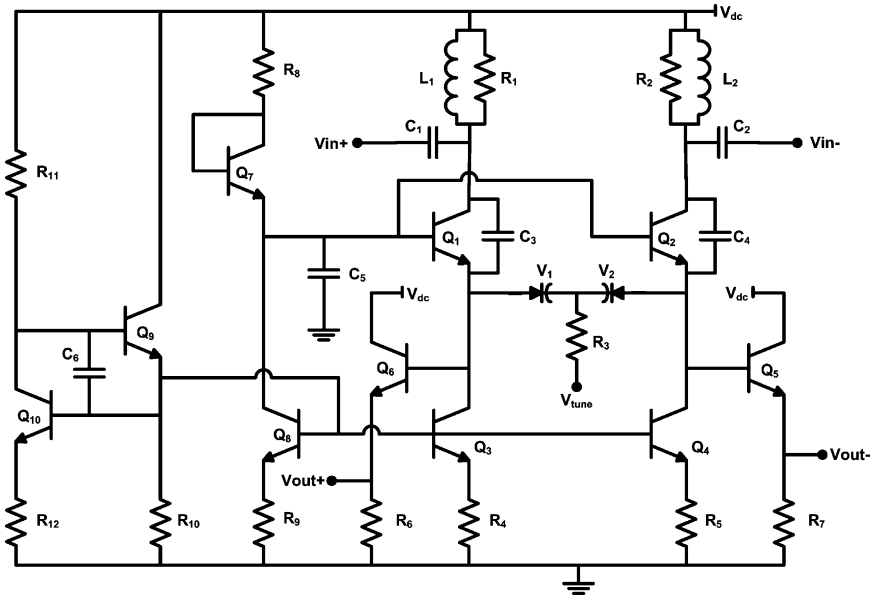

Figure 6. Schematic of the differential input differential output VCILFD.

single-ended or differential-input is appended to inject the reference signal. The multiband operation can be obtained by using switching circuits to select between several VCOs, LC tanks or inductors only. Finally, an output buffer is needed to provide isolation and impedance matching. The complete VCILFD topology shown in Figure 1 includes the core of the VCILFD, broadband output buffers, and the frequency band switching network.

The use of electrical switches, implemented using transistors, PIN diodes or MEMS has been proposed to reconfigure the frequency properties of a VCO. At microwave frequencies, PIN diodes act as variable resistors and offer high current capability and better linearity. High resistance is achieved with no DC current while low resistance is achieved by a high DC current. FET-based switches are preferable as they do not consume DC current while the main limitation is the linearity. Finally, MEMS switches are potential candidates for frequency band selection due to high linearity and low insertion loss. However, the use of such devices increases the cost of the design.

To avoid Q degrading the LC tank, we used PIN diodes for the frequency band switching. As shown in Figure 1, two branches are implemented using PIN diodes and inductors with different values in series with capacitors to block the control voltage. The third one includes only an inductor allowing the bias current to flow. When D_1 and D_2 are not in the active region of operation they approximate an open circuit and the resonant frequency depends on the value of L_3. When D_1 or D_2 is in the active region of operation the corresponding branch presents a low impedance path, and thus, the resonant frequency depends on the parallel combination of L_3 and L_1 or L_3 and L_2, respectively. Consequently, the proposed topology enables three different inductor values to be selected resulting in three different frequency bands. We can observe from Figure 1 that negative power supply and positive control voltages are necessary for the appropriate selective operation. Alternatively, positive power supply can be applied by introducing a different frequency band switching network. Each branch including a PIN diode is replaced with the one shown in Figure 2. Q_7 is used as a current source. It should be noted that in this case the collector-to-emitter parasitic capacitance directly affects the frequency of oscillation and should be taken into account.

The core of the VCILFD is based on the approach originally proposed in [13, 14] and incorporates high-frequency SiGe BJT instead of MOSFET devices. The injected signal is applied to the base of Q_1 and then delivered to the common emitter connection of Q_2 and Q_3. The output and the injection signal are thus summed across the bases and the emitters of Q_2 and Q_3. To achieve broadband impedance matching we use the controllable voltage V_{bias} to set the g_m of Q_5 and Q_6 and thus the output resistance of the buffer.

As we have previously noted, the cross-coupled LC VCO operates at 1.25, 2.5, and 5 GHz, whereas injection locking has been observed when applying 2.5, 5, and 10 GHz resulting in division ratios of 2, 4, and 8 (Table I).

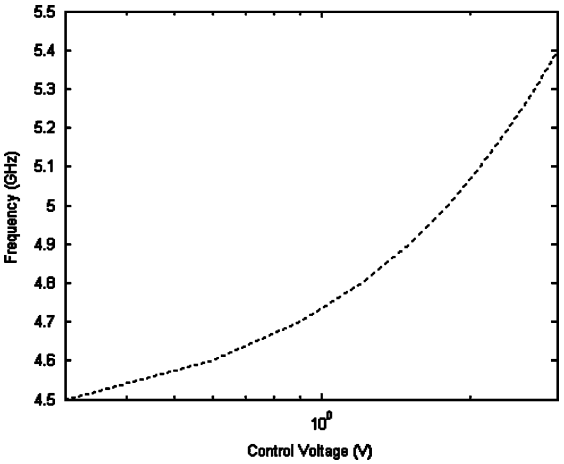

Figure 7. Simulated tuning range of the differential input differential output VCILFD.

Furthermore, the tuning range, obtained by performing a Harmonic Balance simulation in conjunction with a swept variable (Vtune) is: (a) from 1.19 to 1.28 GHz, (b) from 1.9 to 2.75 GHz, and (c) from 4.5 to 5.4 GHz, achieved by a control voltage from 0 to 3 V as shown in Figure 3.

A different architecture shown in Figure 4 is the single-ended input single-ended output. The same frequency band switching network is used except for the different arrangement. The injected signal is applied to the gate of M_1. Like in the previously described scheme, an output buffer is employed, which uses the extra terminal V_{bias2} for better impedance matching in all the different frequency bands, in order to provide more isolation.

The modified Colpitts oscillator operates at 2.5, 5, and 10 GHz, whereas injection locking has been observed when applying 5, 10, and 20 GHz resulting in division ratios of 2, 4, and 8 (Table II).

In this topology, the tuning range at the three different frequency bands is: (a) from 1.9 to 2.8 GHz, (b) from 4.5 to 5.4 GHz, and (c) from 8.9 to 11.4 GHz, achieved by a control voltage from 0 to 3 V as shown in Figure 5.

Last but not least, we introduce a differential-input differential-output VCILFD with a division ratio of 2 operating at 5 GHz. The schematic of the proposed topology is depicted in Figure 6. The injected signal is applied to the collectors of Q_1 and Q_2 while the output signal having a divided by 2 frequency is taken from the emitters of the Q_5 and Q_6 devices which form the output buffers. The input frequency ranges from 9.0 to 10.8 GHz while the output frequency ranges from 4.5 to 5.4 GHz (Figure 7).

2.2. Phase noise and locking range analysis

After a brief introduction to the injection-locked frequency division mechanism, we will introduce a short anal-

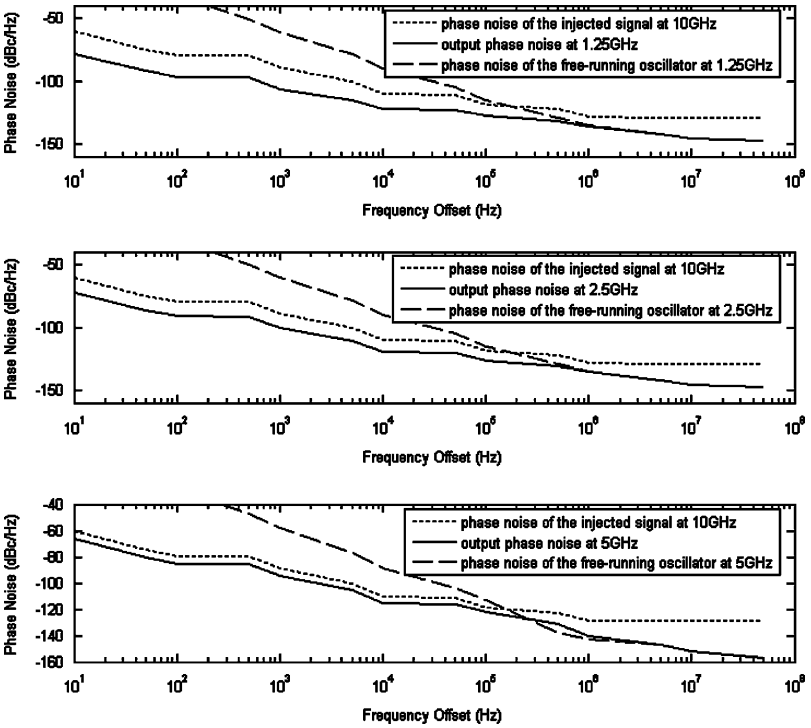

Figure 8. Phase noise simulation results.

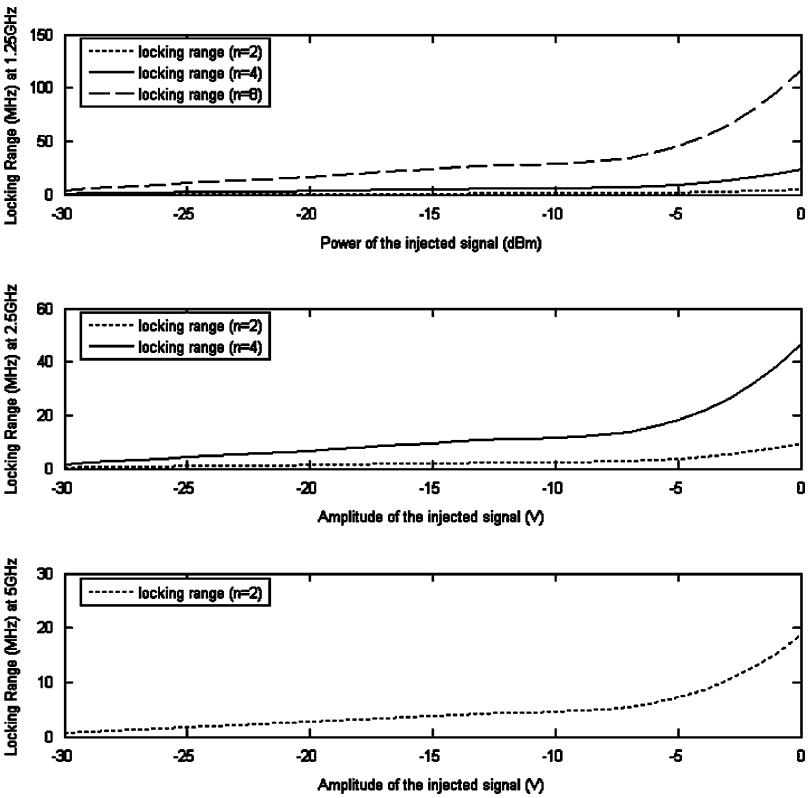

Figure 9. Simulated locking range versus the power of the injected signal.

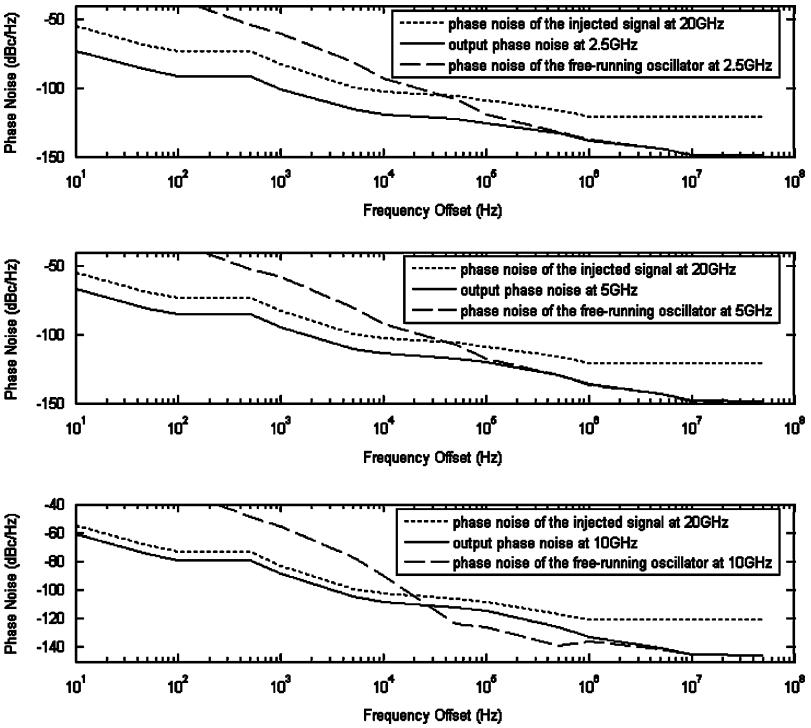

Figure 10. Phase noise simulation results.

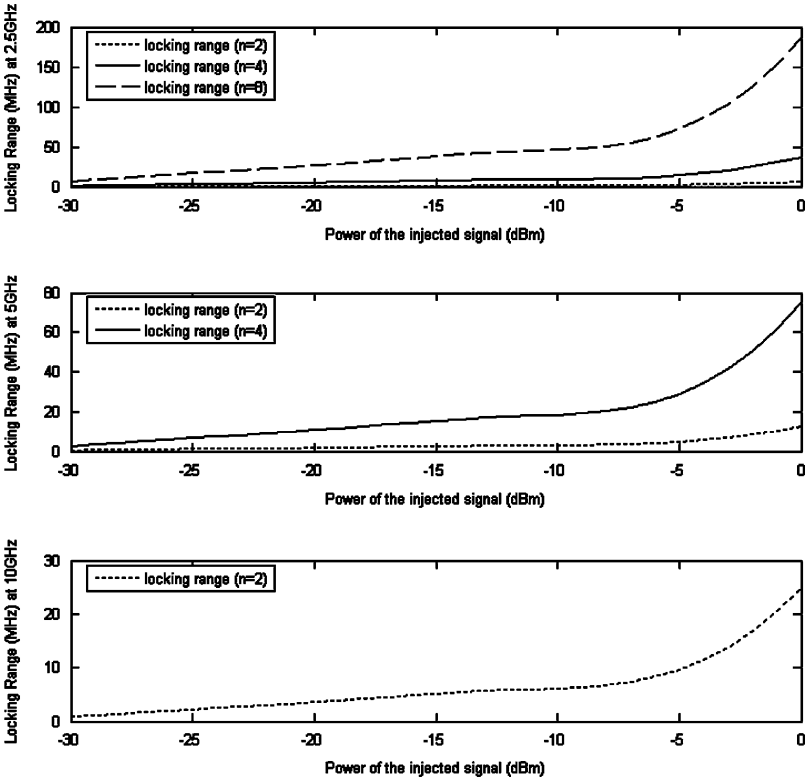

Figure 11. Simulated locking range versus the power of the injected signal.

Table III. Locking range and phase noise measurement results.

	Locking range	Phase noise at 100 kHz offset from carrier (measured)	Phase noise at 100 kHz offset from carrier (calculated)
Modified Colpitts VCO-based VCILFD	1.90–2.75 GHz (:2)		
	1.88–2.81 GHz (:4)		
	1.72–2.99 GHz (:8)	−126 dBc/Hz	−127.8 dBc/Hz
	4.48–5.41 GHz (:2)		
	4.43–5.46 GHz (:4)	−119 dBc/Hz	−120.5 dBc/Hz
	8.88–11.45 GHz	−113 dBc/Hz	−114.8 dBc/Hz
LC cross-coupled VCO-based VCILFD	1.19–1.29 GHz (:2)		
	1.85–2.78 GHz (:4)		
	1.08–1.38 GHz (:8)	−126 dBc/Hz	−127.7 dBc/Hz
	1.88–2.74 GHz (:2)		
	1.85–2.79 GHz (:4)	−125 dBc/Hz	−126.3 dBc/Hz
	4.47–5.41 GHz	−121 dBc/Hz	−122.5 dBc/Hz

ysis for the phase noise performance of the proposed architectures.

Along with the desired oscillating signal, an oscillator typically produces harmonics of the signal due to the nonlinear operation of the active elements. As we have previously described, such an oscillator can be locked to an injected signal (ω_{inj}) whose frequency equals to a harmonic of the oscillator frequency ($n\cdot\omega_0$). In this case, all the produced frequencies including the fundamental one are injection locked to the injected signal. The fundamental oscillator frequency (ω_0) equals the frequency of the injected signal divided by n resulting in a division operation.

Considering the harmonic frequency signal ($n\cdot\omega_0$) as the desired output frequency interacting with the injected signal (ω_{inj}) like in fundamental injection, we can determine the locking range following the method of Daryoush [15]:

$$\Delta\omega_n = \omega_0 - \omega_r = \frac{\omega_0}{2Q}\sqrt{P_{\text{inj}}/P_{\text{harm}(n)}} \tag{1}$$

where ω_r and Q are the resonant frequency and the quality factor of the tank circuit used, P_{inj} is the power of the injected signal and $P_{\text{harm}(n)}$ is the power of the nth harmonic signal.

Thus, the phase noise at the output can be derived by modifying the well-known method for the subharmonic frequency injection [15]:

$$L_{\text{out}}(\omega) = \frac{(1/n)^2\Delta\omega_n^2 L_{\text{inj}}(\omega)\cos^2\varphi + \omega^2 L_{\text{vco}}(\omega)}{\Delta\omega_n^2\cos^2\varphi + \omega^2} \tag{2}$$

where $L_{\text{vco}}(\omega)$ is the single-sideband spectral density of the phase noise of free-running signal while $L_{\text{inj}}(\omega)$ is the single-sideband spectral density of the phase noise of the injected signal. The phase difference φ is expressed in terms of locking range as:

$$\phi = \sin^{-1}\left(\frac{\omega_0 - \omega_{\text{inj}}/n}{\Delta\omega_n}\right) \tag{3}$$

From Equation (2) it is clear that the divider phase noise tracks the phase noise of the incident signal for low-frequency offsets (lower than $((\omega_0/2Q)\sqrt{P_{\text{inj}}/P_{\text{harm}(n)}})$.

Phase noise simulations have been performed using Agilent ADS for the free-running mode of operation and the results together with the phase noise profile of the signal source (obtained by measurement) are substituted into Equation (2) in order to obtain the phase noise at the output of the divider. The simulation results are plotted in Figure 8 depicting the three different frequency bands of operation. The dashed line shows the phase noise of the free running VCILFD while the dotted line is the phase noise of the signal generator used as the injected signal with the frequency doublers connected to the output. Finally, the solid line shows the phase noise of the VCILFD when locked to the injected signal.

Although we have already presented the tuning range of the LC cross-coupled oscillator in Figure 3, it can be further extended by varying the frequency of the injected signal as shown in Figure 9.

Thus, the input/output frequency range when the input power is 0 dBm is defined in Table III.

The phase noise performance of the modified Colpitts oscillator-based VCILFD versus the frequency offset from the 2.5, 5 and 10 GHz carrier is shown in Figure 10. Furthermore, the locking range and the input/output frequency range are defined in Figure 11 and Table III respectively.

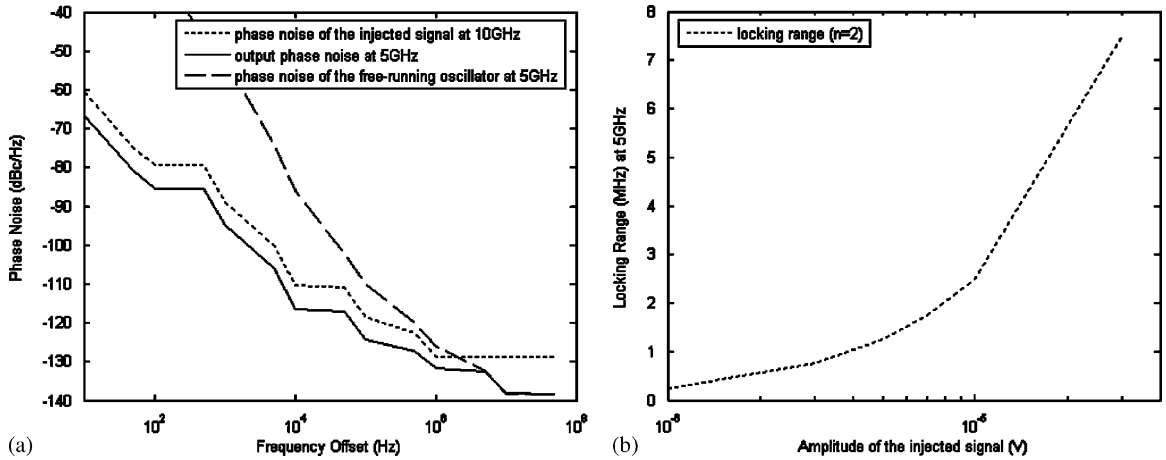

Figure 12. Simulated phase noise (a) and locking range and (b) for the fully differential VCILFD.

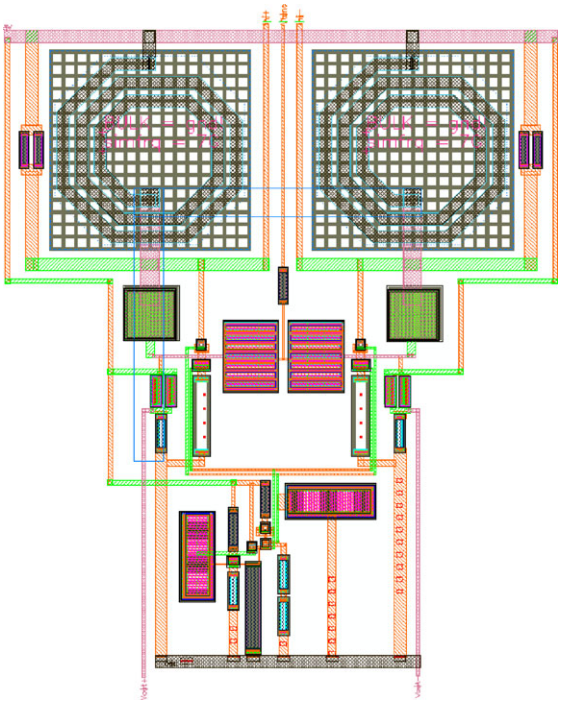

Figure 13. Layout of the fully differential VCILFD.

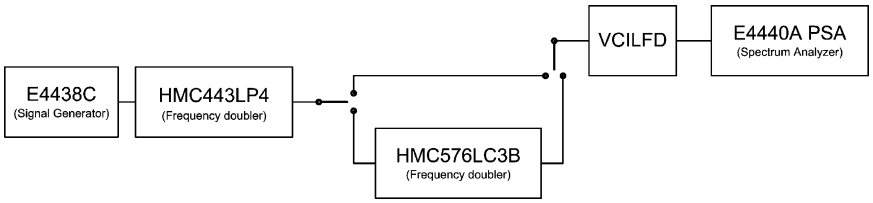

Figure 14. Measurements setup.

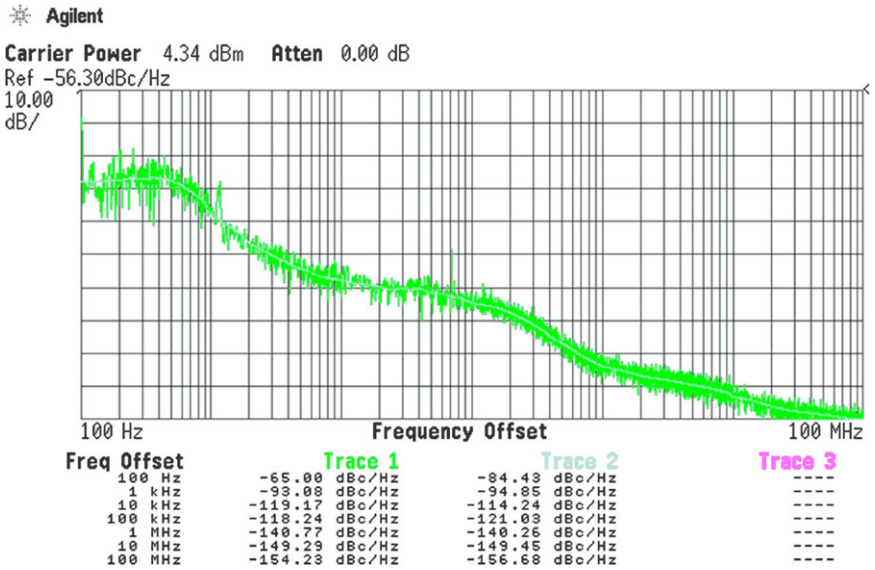

Figure 15. Measured phase noise at the output of the LC cross-coupled VCO-based VCILFD over a broad range of frequency offsets from the 5 GHz carrier (10 GHz input signal).

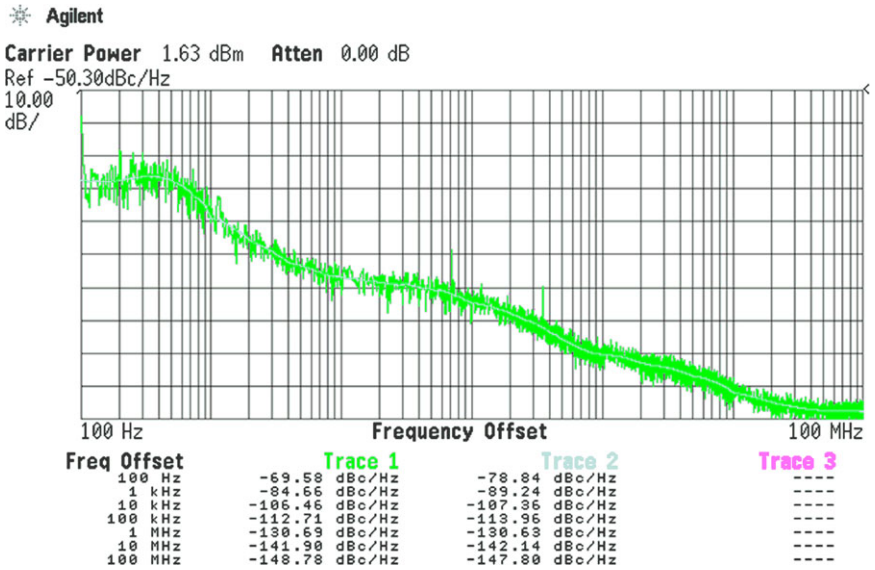

Figure 16. Measured phase noise at the output of the modified Colpitts VCO-based VCILFD over a broad range of frequency offsets from the 10 GHz carrier (20 GHz input signal).

For the fully differential 5 GHz VCILFD the phase noise performance and the locking range are presented in Figure 12(a) and (b), respectively.

As described above the close-in output phase noise of the frequency division output signal is degraded by $20\log(n)$ compared with that of the injection signal as in the conventional frequency division, whereas at high-frequency offsets the output phase noise tracks the phase noise of the free-running oscillator.

3. PERFORMANCE

Discrete versions of the circuits, using the NE3210S01 HJ FET, the NESG2031M05 SiGe RF transistor and the MA46H071 varactor, are designed, and fabricated on a PTFE substrate with a relative dielectric constant of 6.15 and a thickness of 10 mils. The fully differential VCILFD was designed (Figure 13) using a commercial 0.25 µm SiGe BiCMOS foundry process.

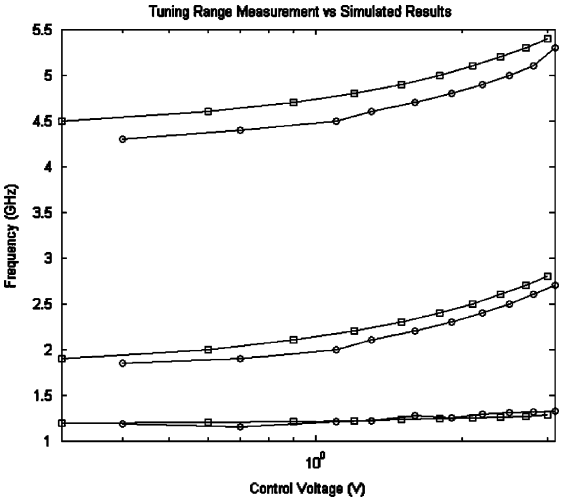

Figure 17. Measured tuning range (solid line with circle marker) and simulated tuning range (solid line with square marker) as a function of the control voltage for the LC cross coupled VCO-based VCILFD.

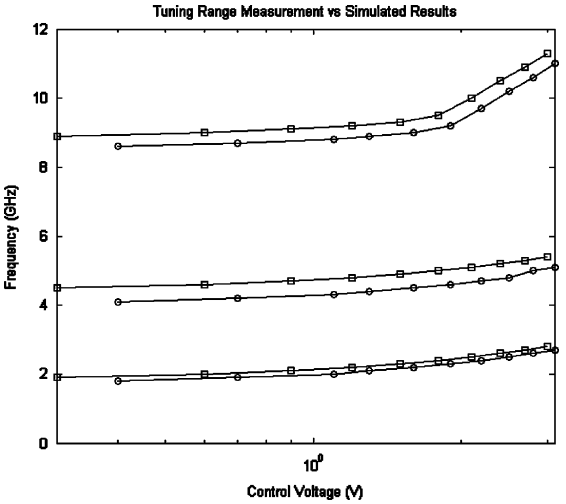

Figure 18. Measured tuning range (solid line with circle marker) and simulated tuning range (solid line with square marker) as a function of the control voltage for the modified Colpitts VCO-based VCILFD.

Measurements are performed using the E4440A PSA (Spectrum Analyzer 3 Hz–26.5 GHz), the E4438C Vector Signal Generator (250 kHz–6 GHz), and frequency doublers (using HMC443LP4 and HMC576LC3B), to produce the injection signals up to 20 GHz. Figure 14 shows the setup for the tuning range, locking range, and phase noise measurements.

The phase noise measurement results for the free running oscillator and the signal generator, with the frequency doublers connected to the output, have already been shown in Figures 8, 10 and 12(a) and used in the analysis presented in Section 2. Moreover, the measured phase noise at the output of the two proposed architectures is presented in Figures 15 and 16 , respectively when the injected signal is -15 dBm.

Finally, in Table III, we summarize the phase noise performance for all the output frequency bands of operation at a frequency offset of 100 kHz from carrier.

The calculated and measured phase noise levels are in relatively good agreement (Table III). For small frequency offsets the output has a $20\log(n)$ better phase noise than the injected signal as expected. This implies that no noticeable phase noise is added during the division process. However, at higher offset frequencies the phase noise tracks the phase noise of the free-running oscillator or becomes even worse due to the excess noise from the divider and the added noise from the output buffer.

The tuning range over which the circuits can be used as frequency dividers is shown in Figures 17 and 18. The experimental measurements verify the theoretical and simulation predictions of the previous sections whereas the locking range is not affected by the changes in the control voltage.

The locking range of the VCILFDs was measured at a power level of 0 dBm and the results are given in Table III. The locking range is almost proportional to the input power and symmetric around the free-running frequency when the input power is small.

For the fully differential VCILFD the post layout simulation matched schematic simulation very well. The phase noise is -114 dBc/Hz at 100 kHz, the tuning range is from 4.28 to 5.3 GHz as the control voltage is increased from 0 to 3 V, and the locking range is from 150 kHz to 5.5 MHz when the input power is varied from -25 to 0 dBm.

The modified Colpitts oscillator-based VCILFD consumes 21 mW under a supply voltage of 3 V, the cross-coupled LC oscillator-based VCILFD draws a dc current of 12 mA from a 3 V supply whereas the fully differential VCILFD is biased with a 3 V supply and the bias current is 5 mA.

4. CONCLUSION

A feasibility study on the application of superharmonic injection locking in frequency division, together with an analysis for the prediction of the phase noise at the output of the proposed circuits has been presented. Three different architectures have been demonstrated: (a) an LC cross-coupled oscillator-based, single-ended input differential-output VCILFD which is functional for input frequencies up to 20 GHz while providing division ratios of 2, 4, 8, (b) a modified Colpitts oscillator-based, single-ended VCILFD, operating at three input frequency bands (2.5, 5 and 10 GHz) with possible division ratios of 2, 4, and 8, and (c) a differential-input differential-output VCILFD having an output frequency range of 4.5 to 5.4 GHz, and a division ratio of 2 (limited by the process technology) which corresponds to an input frequency range of 9.0 to 10.8 GHz. Phase noise calculations and measurement

results attest to the validity of the proposed architectures and theoretical analysis. Finally, the characteristics and the performance of the differential-input differential-output circuit topology prove its suitability to meet the demanding requirements for higher-frequency applications.

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