

LETTER TO THE EDITOR

Phase noise characterization of subharmonic injection locked oscillators

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SUMMARY

In this work we present a detailed study of the phase noise of subharmonic injection locked oscillators (s-ILOs). A new simple and efficient model has been presented for accurately predicting the phase noise of a microwave s-ILO. The validity of the analytical technique is verified with measurement results obtained from a 5-GHz fully differential Colpitts-based s-ILO. The results showed that a phase noise improvement of 12 dB at 1 kHz offset frequency compared to the free-running case can be achieved, whereas the power consumption is 21 mW. Copyright © 2010 John Wiley & Sons, Ltd.

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1. INTRODUCTION

The injection-locked oscillator has the inherent capability of tracking an externally applied signal. This type of oscillator exhibits properties similar to a phase-locked loop. In fundamental locking, the two interacting systems operate at nominally the same frequency, while in the more intricate concept of subharmonic locking, the interaction is between systems whose frequencies are subharmonics of each other.

The subharmonic injection-locked oscillator (s-ILO) approach provides an alternative choice for a high-frequency signal generation and is used for synchronization, amplification, phase shifting, or frequency division. An injection-locked oscillator is obtained by applying an external source to a free-running oscillator. Within the locking range, a phase difference from $-\pi/2$ to $\pi/2$ exists between the reference signal and the locked output signal, as will be described in the next section. A zero-degree phase shift specifies the center of the locking range. This phase relation is used to control the oscillator output frequency to lie at the center of the locking range, counteracting any frequency drift. This allows existing (i.e. 802.11b, 1250 MHz band) oscillator designs to be re-used or shared, thereby reducing the system complexity and silicon area of a multiband transceiver. Moreover, since the phase noise of injected VCO is set by the master oscillator used for injection, power consumption of the 5 GHz generator can be optimized independently of phase noise constraints.

The prospect of using a synchronous oscillator to lock a signal at a subharmonic frequency has been studied widely in the literature [1–5]. A subharmonic injection-locked technique has also

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been proposed as a particular technique for optical synchronization of the remoted local oscillator at microwave and millimeter-wave applications [6, 7]. Recently, a V-band CMOS injection-locked oscillator using fundamental harmonic injection was proposed in [8]. Two CMOS injection-locked oscillators for quadrature generation at radio-frequency are reported in [9] while an integrated coupled oscillator array in SiGe for millimeter wave applications is described in [10]. Finally, in [11] some novel synchronization techniques using injection-locking are presented which can be used for modern communication systems, such as WiMax or UWB applications.

However, the phase noise evaluation for subharmonically injected oscillators is mainly based on experiments and greatly lacks detailed theoretical analysis. Therefore the main target of this work is to address the noise properties of s-ILO. We present a noise model, which is a detailed extension of previously reported work [12]. The theoretical results are confirmed by a series of experiments employing a differential Colpitts-based oscillator implementation. The theoretical model and the resulting phase noise expression have been developed to analyze an injection-locked oscillator, but both can be easily modified to model any injection-locked structure (i.e. divider or multiplier). The resulting calculated phase noise of a single oscillator is in excellent agreement with the rigorous formalism of Zhang *et al.* [13]. Moreover, the modularity of this model makes feasible the analysis of any desired coupling topology, while maintaining the accuracy of the single-oscillator case. More specifically, we describe the phase noise of locking schemes between two oscillators in which the free-running frequency of the injected one is a super-harmonic of the injecting frequency. Furthermore, we present a detailed explanation of the subharmonic locking phenomena and finally, we substantiate our theoretical results by a series of measurements.

The test circuits described in this work are implemented in a 47-GHz, 0.5- μm SiGe BiCMOS technology and consume less than 21 mW of power from a 3.0-V supply. Theoretical analysis of the circuit operation is presented and measurement results validate the design.

This paper is organized as follows. Section 2 presents the injection-locked oscillator noise model together with the phase noise and locking bandwidth analysis. We highlight some of the numerical intricacies we have implemented and go on to analyze the various systems in steps. In Section 3 we present simulation results whereas in Section 4 the implementation details of the differential Colpitts-based injection-locked oscillator are given. Starting with the noise of a single oscillator, we continue to describe the well-known cases of subharmonically injected oscillators. The measurement results to confirm the proposed approach are also included. Section 5 presents our conclusions.

2. PHASE NOISE AND LOCKING BANDWIDTH ANALYSIS

A new analytical formulation for the phase noise calculation of s-ILOs is presented together with the equivalent model for the noise contribution. The analysis is based on the approach given in [12] for fundamental injection-locked oscillators where a discrete MESFET VCO implementation has been used to validate the accuracy of the introduced model. In contrast, we study the noise behavior of subharmonic injection-locked VCOs and the proposed theoretical analysis has been applied (for $/2$ subharmonic injection locking) to a bipolar differential Colpitts oscillator implemented in a 0.5- μm SiGe BiCMOS technology.

As shown in Figure 1, the noise from the tank and the $-G_m$ cell can be represented as a fluctuating admittance $Y_{\text{noise}} = G_{\text{noise}} + jB_{\text{noise}}$. The normalized admittance $Y_n = G_n + jB_n$ is defined with $G_n = G_{\text{noise}}/G_L$ and $B_n = B_{\text{noise}}/G_L$ where G_L is the oscillator load admittance in the free running state. The terms G_n and B_n describe the in-phase (amplitude fluctuations) and the quadrature (phase fluctuations) component of the noise signal, respectively. In the absence of injection $-G_m$ (negative conductance) cancels G_T (loss of the tank) and G_L and the phase noise is given by [12]:

$$|\delta\theta_0|^2 = \frac{|B_n|^2}{(2Q\omega/\omega_0)^2} \quad (1)$$

where ω_0 is the free running frequency and Q is the quality factor of the oscillator.

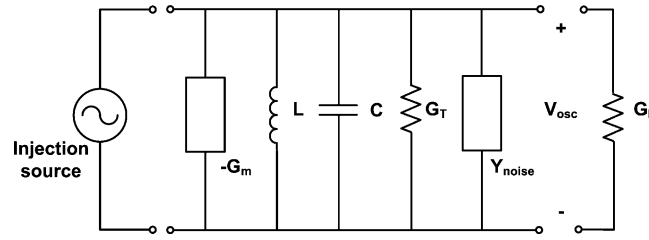


Figure 1. Oscillator model used for the phase noise analysis.

If the oscillator is injection locked to an external signal, the phase relationship between the oscillator and the injection source can be described as

$$\frac{d\theta}{dt} = \omega_0 - \frac{\omega_0}{2Q} \rho \sin(\theta - n\psi_{inj}) - \frac{\omega_0}{2Q} B_n(t) \quad (2)$$

where θ , ψ_{inj} , are the instantaneous phases of the oscillator and the injection signal respectively, ω_0 is the free running frequency, Q is the quality factor of the oscillator, n is an integer representing the subharmonic factor, and ρ is the injection strength. It should be noted that in subharmonic injection ($/n$) the oscillator locks onto the n th harmonic of the injection signal (called synchronizing signal) introduced by the nonlinearities.

If $V_{inj,n}$ is the amplitude of the n th harmonic and V_0 is the amplitude of the free-running oscillator then $\rho = V_{inj,n}/V_0$.

If a steady-state solution can be found such that $d\theta/dt = n\omega_{inj}$, indicating that the oscillator is synchronized to the injected signal, then we have

$$\theta - n\psi_{inj} = \sin^{-1}(\omega_0 - n\omega_{inj}/\Delta\omega_n) \quad (3a)$$

where

$$\Delta\omega_n = (\omega_0/2Q)(V_{inj,n}/V_0). \quad (3b)$$

However, when sinusoidal noise is added both to the oscillator and the injection signal the instantaneous phase of the oscillator and the synchronizing signal will be $\theta + \delta\theta$ and $\psi_{inj} + \delta\psi_{inj}$, respectively (Figure 2). Neglecting the phase perturbation introduced during the harmonic generation process, (2) becomes the perturbed equation:

$$\frac{d\delta\theta}{dt} = -\frac{\omega_0}{2Q} \rho \cos(\theta - n\psi_{inj})(\delta\theta - n\delta\psi_{inj}) - \frac{\omega_0}{2Q} B_n(t). \quad (4)$$

Next, the Fourier transform is calculated to obtain the expression for the total phase noise perturbation:

$$\delta\theta(j\omega) = -\frac{B_n(j\omega)}{j\left(\frac{\omega}{\omega_{3dB}}\right) + \rho \cos(\theta - n\psi_{inj})} + \frac{n\rho \cos(\theta - n\psi_{inj})\delta\psi_{inj}(j\omega)}{j\left(\frac{\omega}{\omega_{3dB}}\right) + \rho \cos(\theta - n\psi_{inj})} \quad (5)$$

where $\omega_{3dB} = \omega_0/2Q$.

Multiplying by the adjoint $\delta\theta^*$, the phase noise spectral density is given by

$$|\delta\theta|^2 = \frac{\left(\frac{\omega}{\omega_{3dB}}\right)^2 |\delta\theta_0|^2}{\left(\frac{\omega}{\omega_{3dB}}\right)^2 + \rho^2 \cos^2(\theta - n\psi_{inj})} + \frac{n^2 \rho^2 \cos^2(\theta - n\psi_{inj}) |\delta\psi_{inj}|^2}{\left(\frac{\omega}{\omega_{3dB}}\right)^2 + \rho^2 \cos^2(\theta - n\psi_{inj})} \quad (6)$$

where $|\delta\theta_0|^2 = |B_n|^2/(\omega/\omega_{3dB})^2$.

To derive the above expression, it has been taken into account that the input noise is uncorrelated with the oscillator noise.

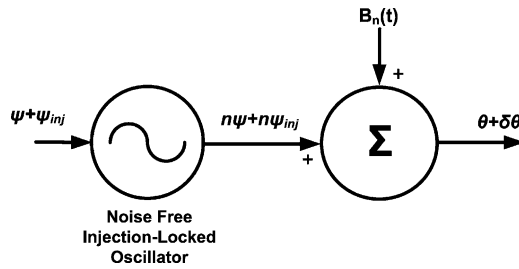


Figure 2. Noise model for deriving the phase noise formula.

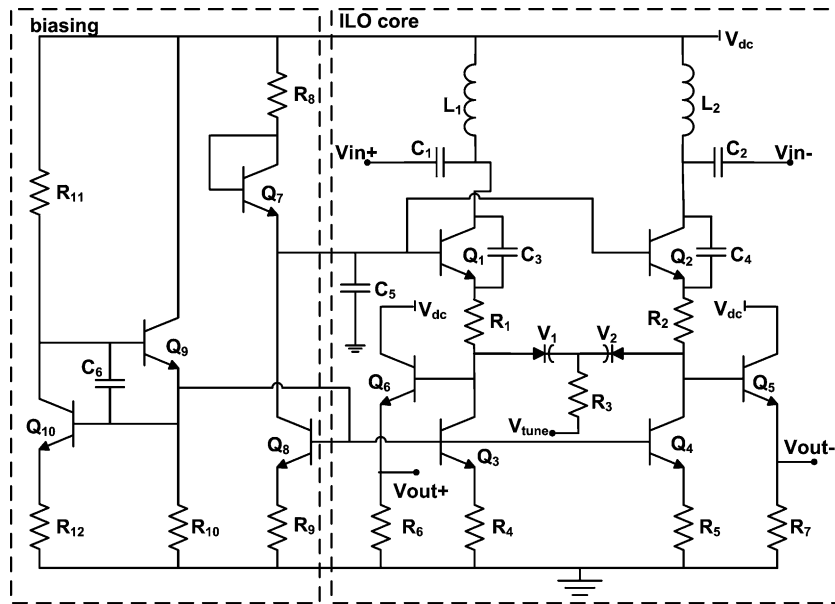


Figure 3. The schematic of the proposed oscillator.

3. SIMULATION RESULTS

A SiGe HBT differential Colpitts oscillator, using the mature BiCMOS 5AM IBM process, was designed based on the single-ended Colpitts oscillator architecture. The selected architecture (Figure 3) incorporates an enhanced biasing scheme and output buffers.

The chosen biasing circuitry is based on an advanced current mirror scheme that is able to provide a temperature-independent current and voltage source to the ILO cell. The proposed structure provides low noise bias current and voltage with constant values that prevents modulation of the oscillation frequency by low frequency noise. The emitter of Q_9 supplies the base currents of Q_{10} , Q_8 , Q_3 , and Q_4 , resulting in an output current I_o much less dependent on β . Using the emitter resistors, any change in the output voltage results in less change in current compared to the current without this feedback which means that the output resistance of the mirror is increased. The effect of mismatch between transistor parameter is also reduced. The simulated temperature coefficient of the proposed current reference is 101.5 ppm/ $^{\circ}$ C, while the load current remains at 3.3 mA for a wide range of load resistances (100–1000 Ω). Finally, simulations show up to 8 dB degradation in the phase noise performance, when the advanced current mirror scheme is not used, due to variations in the bias current.

Output buffers are used to improve the output performance with 50 Ω loads, whereas the VCO is designed to interface with a frequency divider. The supply voltage is 3.3 V.

Although the design of the VCO was not the main target of this work, it was made iteratively according to the following procedure: (a) loop gain analysis, (b) harmonic balance simulation, (c) varactor voltage sweep, (d) phase noise study, (e) layout generation, and (f) redesign after layout. Owing to the parasitic elements introduced by the layout, the design has to start from step (b) again if an increase in phase noise is introduced by the layout step.

Consider the oscillator tank on the left-half side of the oscillator of Figure 3. The oscillator tank consists of the inductor L_1 , the capacitor C_3 and the varactor V_1 . In this case the frequency of oscillation is approximated by

$$\omega_0 = \frac{1}{\sqrt{L_1 \left(\frac{C_3 C_{v1}}{C_3 + C_{v1}} \right)}} \quad (7)$$

where C_{v1} is the capacitance of the varactor V_1 . The oscillator tank is fed back through the emitter of the transistor Q_1 to obtain the oscillator loop. A resistor R_1 is placed before the emitter feedback to further improve the resistive loading of the oscillator tank. In contrast, this resistor will decrease the available voltage drop over the collector-emitter of transistor Q_1 . The lower the voltage drop gets, the more we push the transistor from the saturation region to the active region. We can expect more harmonics and noise in the output of our low noise oscillator. The resistor R_1 is found to have an optimal value of 20Ω in this architecture. The value of C_3 was found to be 1.5 pF , such that the oscillation condition can be satisfied. Proper choice of the passive components for the LC tank will result in the highest possible Q at 5 GHz . It is well known that there is a trade-off between the maximum Q of a given inductor and the frequency of operation and for our case, an inductance value of 1 nH gave the highest Q in combination with the chosen C_1 and C_{V1} values.

Phase noise simulations were performed with SpectreRF including all on-chip parasitics. The resulting phase noise plot is shown in Figure 4, whereas the tuning range of the VCO is $4.9\text{--}5.1 \text{ GHz}$, i.e. 200 MHz . The layout effect causes a small decrease in the oscillation frequency and in the buffer output voltage due to the parasitic capacitances. These performance limitations were taken into account through the design procedure by inserting ideal capacitances of 10 fF at the critical nodes of the design. The buffer output stage is loaded by an ideal capacitance of 200 fF which represents the output RF PAD capacitance (80 fF , $50 \mu\text{m} \times 50 \mu\text{m}$) and ESD assembly. In practice, all the limitations caused by the layout effect can be fully compensated. The decrease in the oscillation frequency (approximately 250 MHz for parasitic capacitances of 10 fF) can be fully compensated by the bondwires inductance since the oscillator resistive load is placed in series with an inductance of at least 1 nH , thus an inductive peaking load is achieved and the oscillation frequency is increased. The voltage drop at the buffer output at high frequencies (60 mV max) can be compensated by an inductor implemented by a bondwire. Further increase of this bondwire inductance can cause higher overshoot at high frequencies which increases the output voltage swing as well and limits adequately the overall output voltage modulation.

A general equation for the phase noise of the s-ILO locked at the n th subharmonic frequency can be derived directly from (6). Thus,

$$L_{\text{ILO}}(\omega) = \frac{n^2 L_{\text{REF}}(\omega) \left[\frac{\omega_0}{2Q} \frac{V_{\text{inj},n}}{V_0} \right]^2 \cos^2 \varphi + \omega^2 L_{\text{VCO}}(\omega)}{\left[\frac{\omega_0}{2Q} \frac{V_{\text{inj},n}}{V_0} \right]^2 \cos^2 \varphi + \omega^2} \quad (8)$$

where φ is the stationary phase difference between the oscillator and the n th harmonic of the reference signal, ω is the offset carrier frequency, ω_0 is the free-running frequency, Q is the quality factor of the embedding network, V_0 is the amplitude of the free-running signal, and $V_{\text{inj},n}$ is the amplitude of the n th harmonic of the reference signal at the output of the oscillator. $L_{\text{VCO}}(\omega)$ is

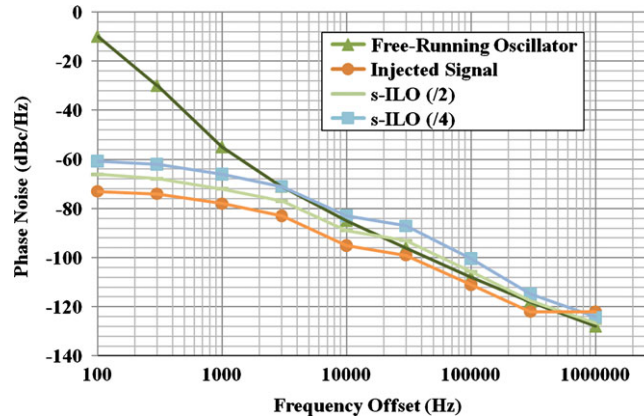


Figure 4. Simulated (free-running case) and calculated phase noise versus offset frequency at the output of the s-ILO.

the single-sideband power spectral density of the phase noise of the free-running oscillator and $L_{REF}(\omega)$ is the single-sideband power spectral density of the phase noise of the reference signal. The angle φ is expressed as

$$\sin \varphi = 2Q \frac{\omega_0 - n\omega_{REF}}{\omega_0} \frac{V_0}{V_{inj,n}} \quad (9)$$

where ω_{REF} is the reference frequency.

The phase noise spectral density of the injection signal obtained from measurements and the VCO obtained from harmonic balance simulations were used in (8) to calculate the total output phase noise at the output of the s-ILO as shown in Figure 4 for $V_{inj,n}/V_0 = 0.06$ and $\cos \varphi = 1$. The locking bandwidth predicted from (3b) is 1.02 and 0.5 MHz when subharmonic injection locking of factor $n = 2$ and $n = 4$ is used, respectively.

4. IMPLEMENTATION AND MEASUREMENT RESULTS

Full-chip, post-layout simulation with extracted parasitic components has been performed, using Cadence Design Framework, to accurately analyze each of these effects. Owing to the presence of a large amount of parasitics, it is important to extract appropriate parasitics for the relevant process corners and perform the analysis. The most critical part is the parasitic capacitance of the interconnection line between the capacitors and the inductors. Without compensation, the parasitic capacitance of the interconnection lines caused a frequency shift of 250 MHz. The proper line width and symmetric layout optimization result in a limited frequency shift of only 65 MHz and it was taken into account when we designed for the center frequency and tuning range of the VCO. A symmetric layout of our differential VCO gave minimum amplitude shifts at the measured output ports. The dimensions of the VCO layout are $0.4 \times 0.4 \text{ mm}^2$ (Figure 5). The longest interconnection between two parts on-chip is only $342 \mu\text{m}$. The parasitic inductances at 5 GHz caused by these short interconnects could be neglected in comparison to the parasitic capacitances.

A comparison of the phase noise simulation results with the measurement results of the free-running VCO is presented in Figure 6. Moreover, the measured phase noise results for the (/2) and the (/4) subharmonic injection are shown in Figures 7(a) and (b), respectively, whereas, all the experimental results are summarized in Table I. The remarkably good agreement with simulation and calculation results validates our approach and confirms the proposed model. The maximum difference between them was 1.5 dB except for the 1–3 kHz range (/4 subharmonic injection) where the deviation is almost doubled. This is due to the smaller amplitude of $V_{inj,4}$ (amplitude

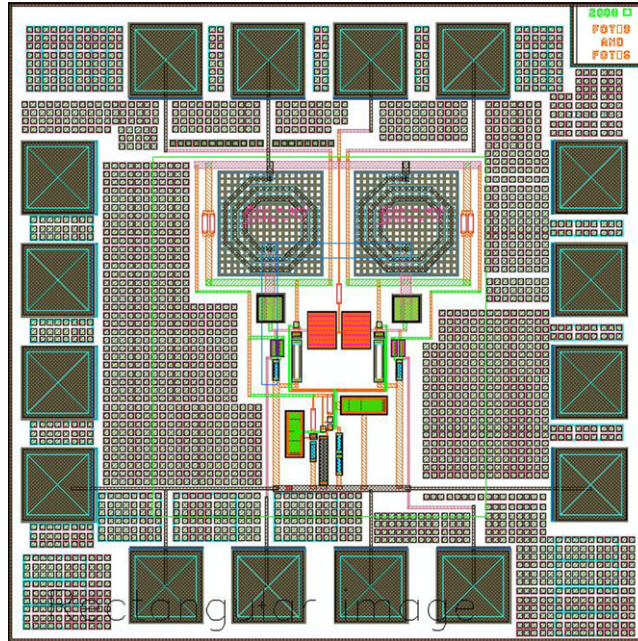


Figure 5. The layout of the proposed s-ILO.

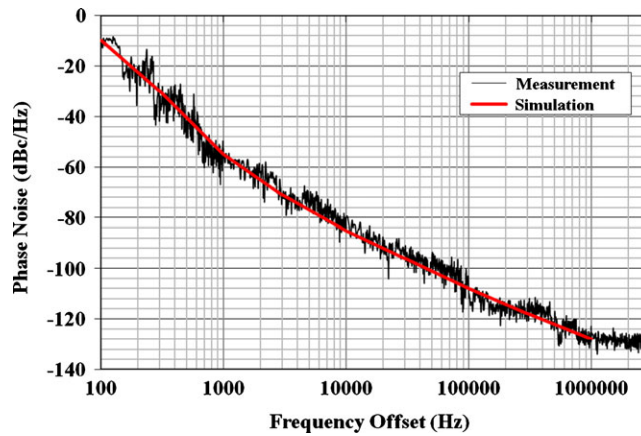


Figure 6. Phase noise simulation and measurement results versus offset frequency.

of the fourth harmonic) with respect to the estimated one. Finally, Table II shows the comparison with previously reported works regarding the phase noise profile estimation.

5. CONCLUSIONS

An analytical method to formulate the injection-locking phenomenon and the phase noise for BJT differential oscillators has been presented. We have expanded a previously developed noise model into a generic one (applicable to the subharmonic case) which can be used to analyze any locked oscillator configuration. We demonstrated this concept by fabricating a differential Colpitts-based

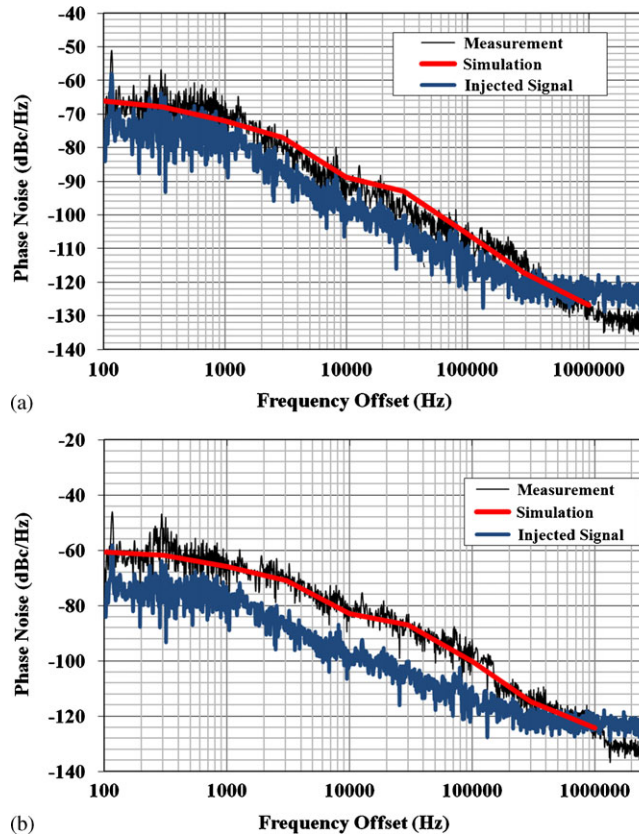


Figure 7. (a) Phase noise versus offset frequency at the output of the s-ILO ($/2$) and (b) phase noise versus offset frequency at the output of the s-ILO ($/4$).

Table I. Summarization of the measurement results.

Parameter	Value (meas./sim.)	Unit
$N = 2$		
Input frequency	2482–2587*	MHz
Output frequency	4964–5156*	MHz
Tuning range	$190 \pm 1^*$	MHz
Phase noise	$-70@1\text{ kHz} / -72@1\text{ kHz}$	dBc/Hz
$N = 4$		
Input frequency	1241.125–1288.875*	MHz
Output frequency	4964.5–5155.5*	MHz
Tuning range	$190 \pm 0.5^*$	MHz
Phase noise	$-65@1\text{ kHz} / -66@1\text{ kHz}$	dBc/Hz
Power consumption	21*	mW
Output power	0/+1.5	dBm
Area	0.16	mm ²
Free-running frequency	4900–5100/4964–5156	MHz

*Input signal dependent.

VCO at 5 GHz. According to the measurement results on the fabricated s-ILO in 0.5- μm BiCMOS process, a phase noise improvement of up to 12 dB with respect to the free-running phase noise is observed at 1 kHz frequency offset for the ($/2$) subharmonic case. This result is in good agreement with theoretical predictions indicating the effectiveness of the proposed formulation.

Table II. Performance summary.

	Phase Noise (dBc/Hz)		Injection locking type	Free-running freq. (GHz)
	$\omega < \omega_L$	$\omega > \omega_L$		
[12]	-70@100kHz	-90@1MHz	Fundamental ($F_{out} = F_{in}$)	8.5
[13]	-108+20log ₁₀ 4@100kHz -108+20log ₁₀ 3@100kHz -108+20log ₁₀ 2@100kHz	-105@1MHz	Subharmonic ($F_{out} > F_{in}$)	5.0
[14]*	-124+20log ₁₀ 16@100kHz	—	Subharmonic ($F_{out} > F_{in}$)	8.0
[15]	-80+20log ₁₀ (1/2)@100kHz	-125@10MHz	Super-harmonic ($F_{out} < F_{in}$)	1.88
[16]	-90+20log ₁₀ (1/2)@100kHz	-115@10MHz	Super-harmonic ($F_{out} < F_{in}$)	2.7
[17]†	-130+20log ₁₀ 5@100kHz	—	Subharmonic ($F_{out} > F_{in}$)	5.0
This work	-112+20log ₁₀ 2@100kHz -112+20log ₁₀ 4@100kHz	-124@1MHz	Subharmonic ($F_{out} > F_{in}$)	5.0
Phase noise profile	$L_{REF} + 20 \log_{10} N$	L_{VCO}	All cases	

ω_L , lock range; L_{REF} , phase noise of the reference signal; L_{VCO} , phase noise of the free-running VCO; N , F_{out}/F_{in} .

*Experimental results only.

†No theoretical analysis for the s-ILO.

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