Computers and Electrical Engineering xxx (2012) xxx–xxx

Contents lists available at SciVerse ScienceDirect

Computers and Electrical Engineering

journal homepage: www.elsevier.com/locate/compeleceng

A 1 GHz, DDR2/3 SSTL driver with On-Die Termination, strength calibration, and slew rate control

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ARTICLE INFO

Article history:
Received 5 August 2011
Received in revised form 29 December 2011
Accepted 29 December 2011
Available online xxxx

ABSTRACT

A 1 GHz Double Data Rate 2/3 (DRR2/3) combo Stub Series Terminated Logic (SSTL) driver has been developed for the first time to our knowledge using a 90 nm CMOS process. To satisfy the signal integrity requirements the driver strength is dynamically calibrated and the input/output port is efficiently terminated by on-die resistors. Furthermore, the slew-rate can be sufficiently controlled by selecting an appropriate external resistor. The proposed driver design provides all the required output and termination impedances specified by both the DDR2 and DDR3 standards and occupies a small die area of 0.032 mm^2 (differential). Experimental results demonstrate its robustness over process, voltage, and temperature variations.

1. Introduction

1.1. The demand

The demand for memory systems with data rates of over 1-Gb/s is continuously increasing during the last 5 years [1,2]. This is achieved through the use of DDR3 memory modules which enable higher bus rates and peak rates than earlier memory technologies, and thus, it is important to get the maximum benefit from this new standard while at the same time being able in reusing the existing DDR2 memory interface designs.

1.2. The challenge

DDR3 Synchronous dynamic random access memory (SDRAM) consists of a merged driver that is a combination of an output driver and a termination driver. Multiple 240 Ohm structures are used to enable pull-up and pull-down drivers which provide all the required termination values, using combinations of the same pull-up and pull-down driver legs. The full-strength driver has an output impedance of 34.3 Ohm, derived by activating seven 240 Ohm pull-up and pull-down legs. This merged driver reuses portions of the output driver structure for implementing the termination values and thus the input capacitance of the driver is reduced [3]. The optimal termination value for the DDR3 memory module that is being accessed during a write command is a high-impedance value of about 60 or 120 Ohm while low-impedance values, such as 30 or 40 Ohm are also available. On the other hand, the optimum output impedance value for an SSTL DDR2 driver is 18 Ohm and the termination resistance values are 150, 75 and 50 Ohm. It is clear from the above discussion that there is no common impedance ratio between the two schemes and thus it is difficult to implement a combined (combo) DDR2/DDR3 SSTL driver.

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doi:10.1016/j.compeleceng.2011.12.012

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1.3. Literature review

Various SSTL topologies, mainly as parts of dynamic random access memory (DRAM) devices or DDR memory interfaces, have been proposed. In [4], a DDR2 SDRAM is presented incorporating On-Die Termination (ODT) and Off-Chip Driver calibration (OCD). The ODT can provide either 150 or 75 Ohm values depending on the system configuration. Regarding OCD calibration, the output driver strength is controlled to be 18 ± 3 Ohm by a chipset whereas in [5] the output circuit of the 512-Mb DDR2 SDRAM presented, reduced the output skew by adjusting the impedance and slew-rate. Three circuit techniques for a DDR1/DDR2 compatible chip architecture designed for both high-speed and high-density DRAMs are described in [6], where furthermore, a DDR1/DDR2 compatible hybrid multi-oxide output buffer is proposed. In [7], the implementation of a 512-Mb DDR3 SDRAM prototype is presented. The output driver comprises an active device (MOS transistor) and passive device (resistor), which are serially connected to each other. In [8] the design of a CMOS I/O driver that is less sensitive to process-voltage-temperature (PVT) variations is presented. The proposed driver achieves lower PVT sensitivity by flattening its output resistance response, thereby obtaining better output impedance matching. In [9], a CMOS Decision Feedback Equalizer (DEF) receiver was implemented and applied to the receiver side of an SSTL DRAM interface. In [10], a new termination set is proposed to support the DDR3 – static random-access memory (SRAM) mode. A programmable impedance controller (PIC) creates the impedance codes, having as reference the external resistors R_T and R_Q for ODT and OCD, respectively. In [11] a 1.2-V 1.5-Gb/s 72-Mb DDR3 SRAM is described, which satisfies the need for high data rate and area density required in recent ultra fast systems together with the corresponding on-chip termination. In [12] the implementation of a third-generation 1.1-GHz 64-bit microprocessor is presented whereas it provides some details on the DDR1 SSTL I/O circuit solutions at the memory interface. Finally in [13], a DDR2 memory interface is proposed, where the SSTL driver is implemented using a DDR3 architecture. Regarding commercial solutions, Synopsys' Designware IP DDR multiPHY [14], supports a wide range of DDR SDRAM types. This allows the host SoC/ASIC to be easily configured according to the requirements of the specific DDR SDRAM variant used in the system, via simple software control allowing one chip to target multiple applications by using different DDR types.

1.4. Differentiation

In this paper, in contrast to the above mentioned schemes which focus on DDR2 or on DDR3 I/O architectures and relevant optimizations but not on combination of them, we present the first 1 GHz combo DDR2/3 SSTL driver implementation to our knowledge, in the sense that it achieves both the 1.8 V DDR2 and the 1.5 V DDR3 operations according to the corresponding JEDEC standards [15–17] using a common architecture. Furthermore, control of slew rate along with ODT and OCD calibration at either the rails (VDDQ/VSS) or at VDDQ/2 are supported which forms an addition point of differentiation. The validity of the proposed scheme has been verified through simulation (using appropriate modeling and methodology [18,19]) and experimental results. The simulation environment of our test chip included a memory interface verification IP with real memory models. This combined driver is a DDR2/3 SSTL driver optimized in terms of area and performance characteristics which is ideal for designers who are currently implementing DDR2 interfaces and would like to have the option of migrating to DDR3 ones when they become more cost effective, as well as for use in today's combo DDR2/3 memory interface solutions.

This paper is organized as follows. In Section 2 we analyze the selection and the design of the specific SSTL topology, while various design trade-offs are discussed. In Section 3 we describe the overall implementation together with experimental results meeting the requirements of JESD8-15A, JESD79-2F and JESD79-3E. Finally, we provide our conclusions in Section 4.

2. DDR2/3 compatible SSTL architecture

A block diagram of the proposed DDR2/3 compatible SSTL driver is presented in Fig. 1. The main building blocks include the output driver/termination driver (implemented into the Transmitter/Termination module), the input buffer (implemented into the receiver module), and the Calibration Mechanism. The Transmitter/Termination block provides 1.8 V for

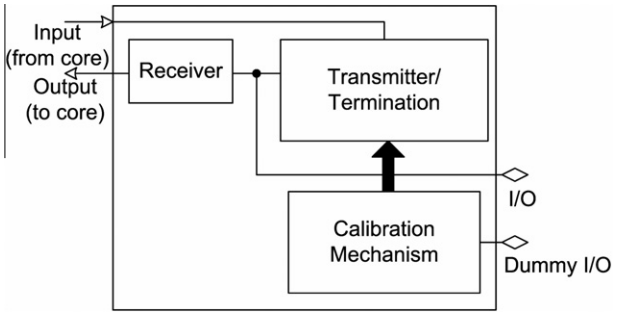

Fig. 1. The block diagram of the proposed DDR2/3 compatible SSTL driver.

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DDR2 operation (1.5 V for DDR3 operation) for data in = '1" and 0 V for data in = "0" along with the appropriate termination values which are 50, 75 and 150 Ohm for DDR2 operation and 30, 40, 60, and 120 Ohm for DDR3 operation, respectively. The differential input buffer (receiver) translates the SSTL input voltage levels to 0–1 V CMOS levels, and also ensures that the output signal has sufficiently fast rise and fall time when applied to the CMOS core. Finally, the impedance of the driver leg is adjusted properly in an automatic way (150/240 Ohm) to account for process, voltage and temperature variations through the employment of the calibration mechanism.

The proposed architecture for the merged output driver/termination driver is shown in Fig. 2. It consists of eight identical submodules (eight p- and n-type legs) where each of them could provide a resistance of either 150 or 240 Ohms, the selection of which depends on whether a DDR2 or DDR3 operation is desirable. Specifically, if DDR2 functionality is required, the full strength driver is formed by enabling all eight 150 Ohm p- and n-type legs exhibiting an output impedance of 18.75 Ohm, while in the DDR3 case seven 240 Ohm p- and n-type legs need to be activated so as to satisfy the requirement that the full strength output impedance be 34.3 Ohm.

An extra couple of p- and n-type legs of 300 Ohm resistance each is used to achieve the 150 Ohm termination value needed in DDR2 operation. Furthermore, in order to minimize the crowbar current through the output transistors, a "break-before-make" predriver circuitry (BbM) is employed [20]. The crowbar (overlap) current is reduced from 20.83 mA (DDR2) and 11 mA (DDR3) to less than 19.5 mA (DDR2) and 10.24 mA (DDR3) respectively when the "break-before-make" mechanism is enabled.

Figs. 3 and 4 show the schematics of the n- and p-type legs, respectively. The DDR2/DDR3 operation is obtained by selecting the appropriate resistor values in all the p- and n-legs (150 or 240 Ohm). Instead of using a simple resistor to achieve that [3,21], a resistor selecting circuit has been employed, comprised of a resistor (R_2) in parallel with a transmission gate and another resistor (R_1) which are connected in series. For DDR2 operation, the sel_1 signal is high and the complementary

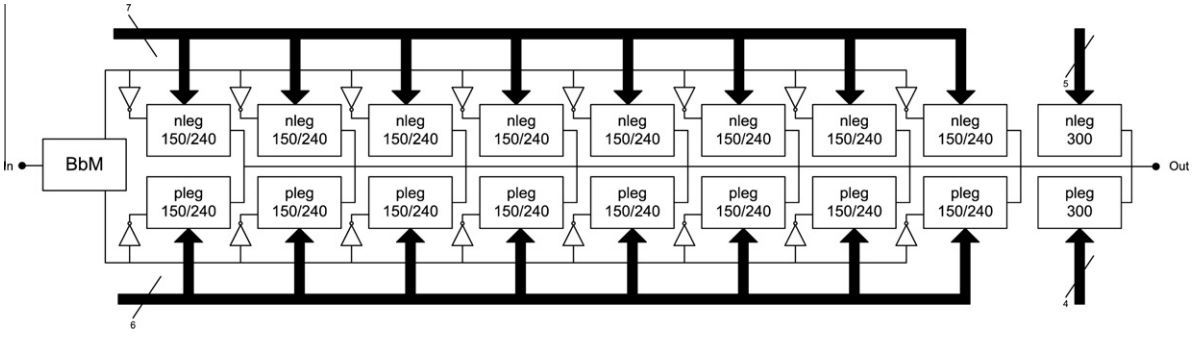

Fig. 2. Block diagram of the proposed DDR2/DDR3 merged driver.

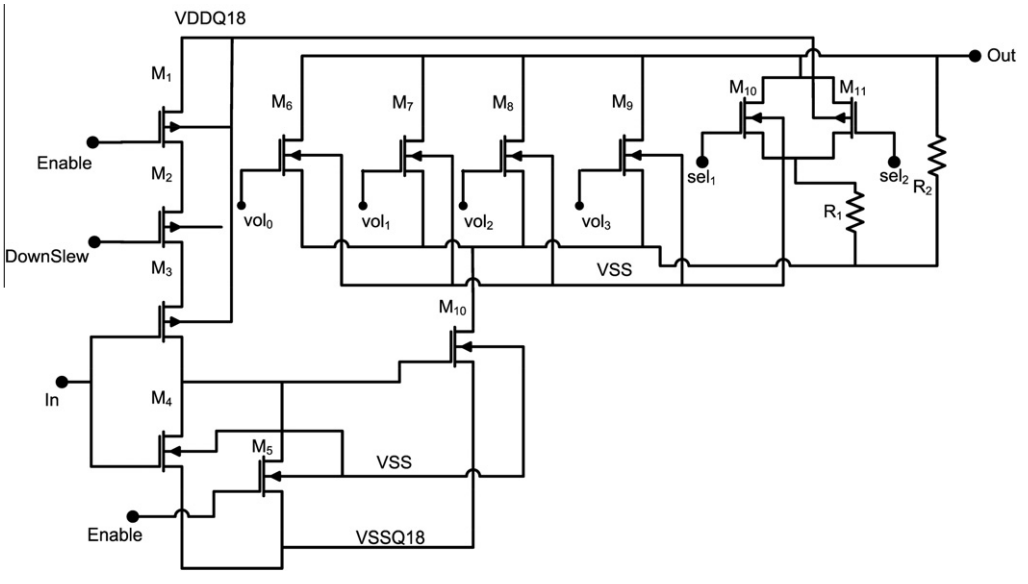

Fig. 3. The n-leg of the proposed output driver/termination driver.

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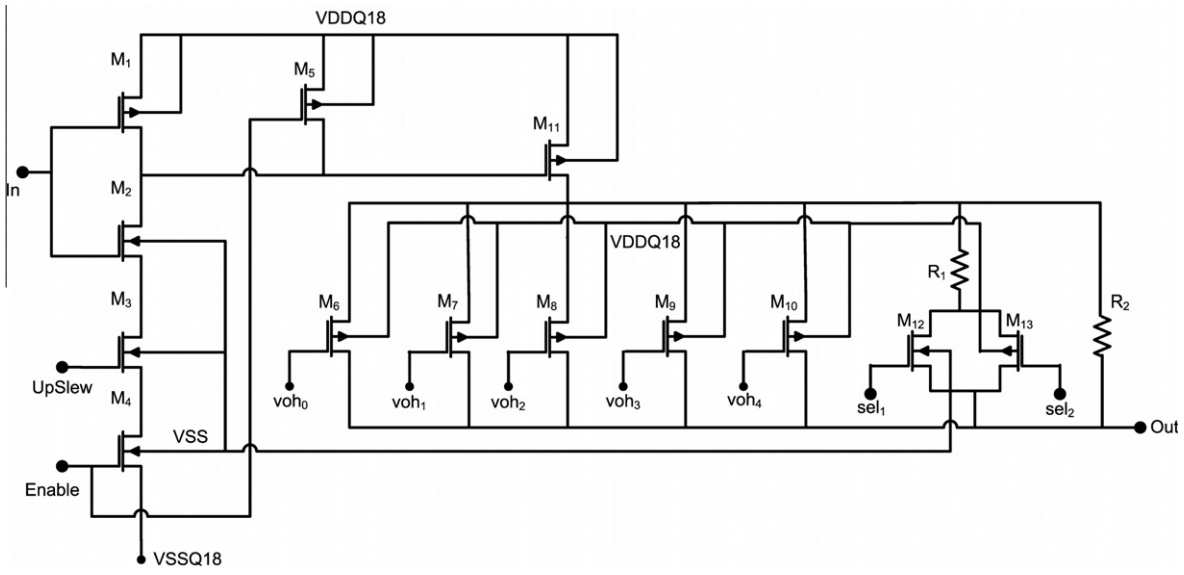

Fig. 4. The p-leg of the proposed output driver/termination driver.

sel_2 signal is low, the transmission gate is on, and thus the total resistance of the selecting circuit is approximately 180 Ohm, i.e. $(R_1 + R_{TG})//R_2$. When the sel_1 signal is low and the complementary sel_2 signal is high, the transmission gate is off, and thus the total resistance of the selecting circuit is approximately 280 Ohm, i.e. R_2, as required for DDR3 operation. The pull-up leg (pleg) has five p-channel devices to adjust the total resistance of the leg and provide a tuning range sufficiently large to compensate for any process, voltage and temperature (PVT) variations. Thus, the total resistance of the leg can be always tuned to the desired 240 or 150 Ohm value. The pull-down leg (nleg) is similar to the pull-up one except for the fact that is using 4

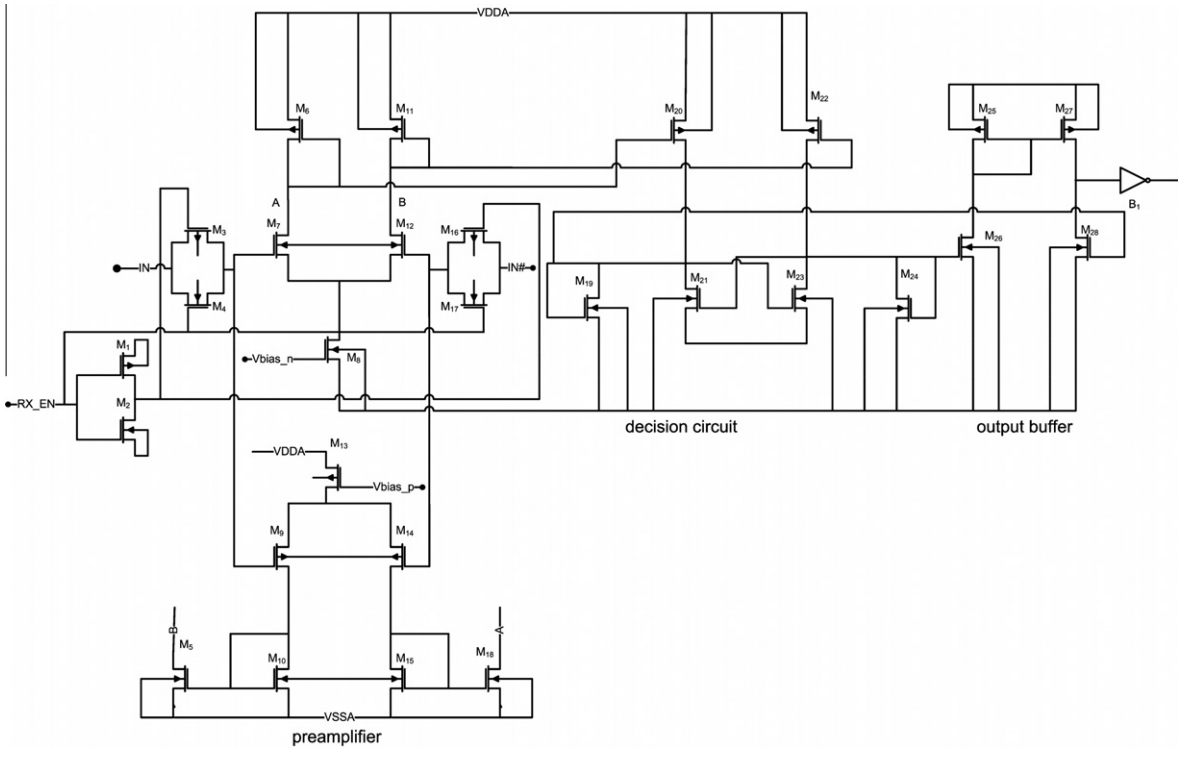

Fig. 5. The proposed input driver.

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n-channel devices due to the different R_{ON} resistance of the P-MOS and N-MOS devices. The 300 Ohm p- and n-legs are designed accordingly using a simple 320 Ohm passive resistor without using the selecting circuit.

The slew rate can be controlled by coordinating the slope of the gate signal of the main driver (i.e. M_{11} for the p-leg or M_{10} for the n-leg). The slew-rate control signals UpSlew and DnSlew are generated simply by using a voltage divider formed by an internal and an external resistor. The value of the external resistor is chosen such that the resultant UpSlew or DnSlew signals provide the desired slew rate.

The schematic of the proposed input buffer is shown in Fig. 5. It consists of three stages: the rail-to-rail preamplifier, the decision stage and the output buffer [22]. The preamplifier consists of both a PMOS and NMOS differential amplifier whereas the decision circuit uses positive feedback from the cross-gate connection of M_{21} and M_{23} to increase the gain of the decision

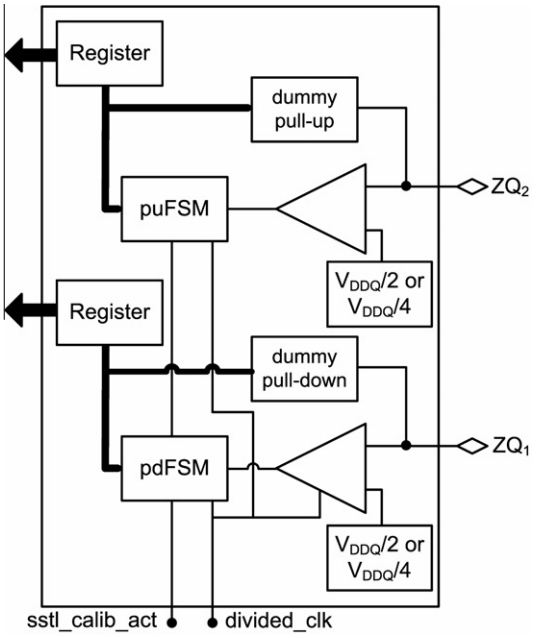

Fig. 6. Termination resistance calibration mechanism.

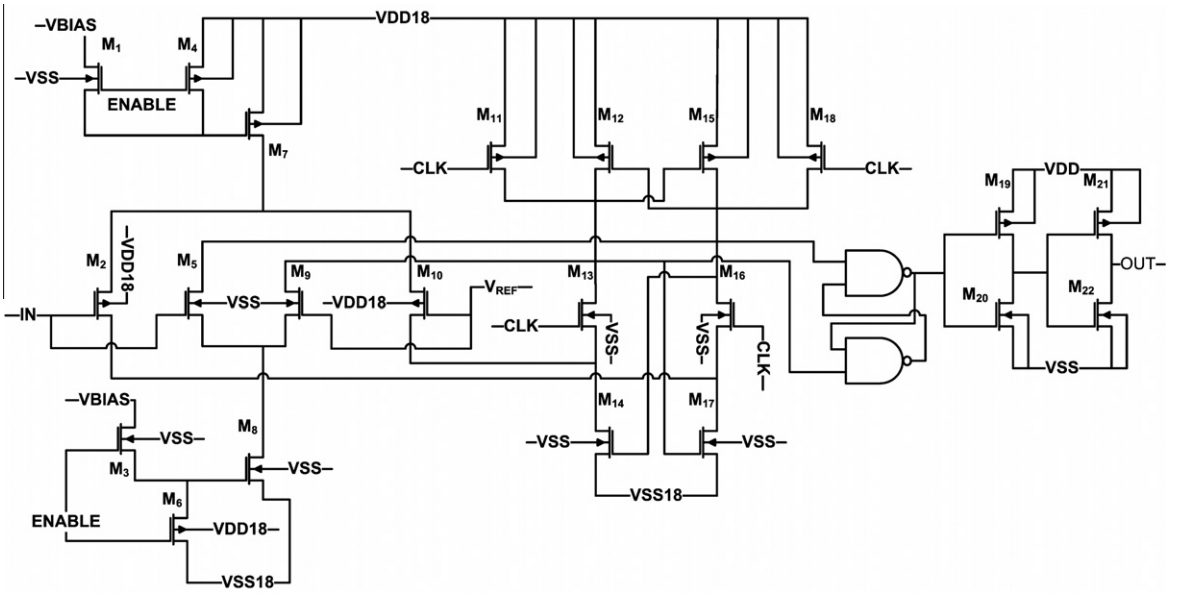

Fig. 7. The clocked comparator.

element. The output buffer converts the output of the decision circuit into a logic signal, and includes an inverter as an additional gain stage as well as to isolate any load capacitance.

The proposed calibration scheme uses two external precision resistors (R_{ZQ}) and is shown in Fig. 6. The main concept is that the resistance of a dummy n-leg and a dummy p-leg of the output driver including the selecting circuit and the combination of transistors is compared to the external resistor R_{ZQ} (240 or 150 Ohm). This is performed by comparing the actual voltage at the ZQ_1 and ZQ_2 points to an internally generated reference voltage, VDDQ/2 (or VDDQ/4), through the use of the comparator shown in Fig. 7. Resistors R_{ZQ} are placed between the ZQ_1 pin and power and between the ZQ_2 pin and ground. The transistors at the legs are binary weighted to provide a resolution of 2% of R_{ZQ}. A 5-bit (*Voh*) and a 4-bit (*Vol*) digital code are used to select or deselect the p-channel and the n-channel devices respectively.

The calibration process of the SSTL I/O involves the execution of two separate binary search algorithms, one for the pull-up and one for the pull-down resistor networks of the SSTL. A successive approximation procedure is implemented by these algorithms performed by two finite state machines (FSMs) which run sequentially, with the pull-down FSM (pdFSM) executing first. As seen from the outside world, the two FSMs operate as a single machine with the activation input

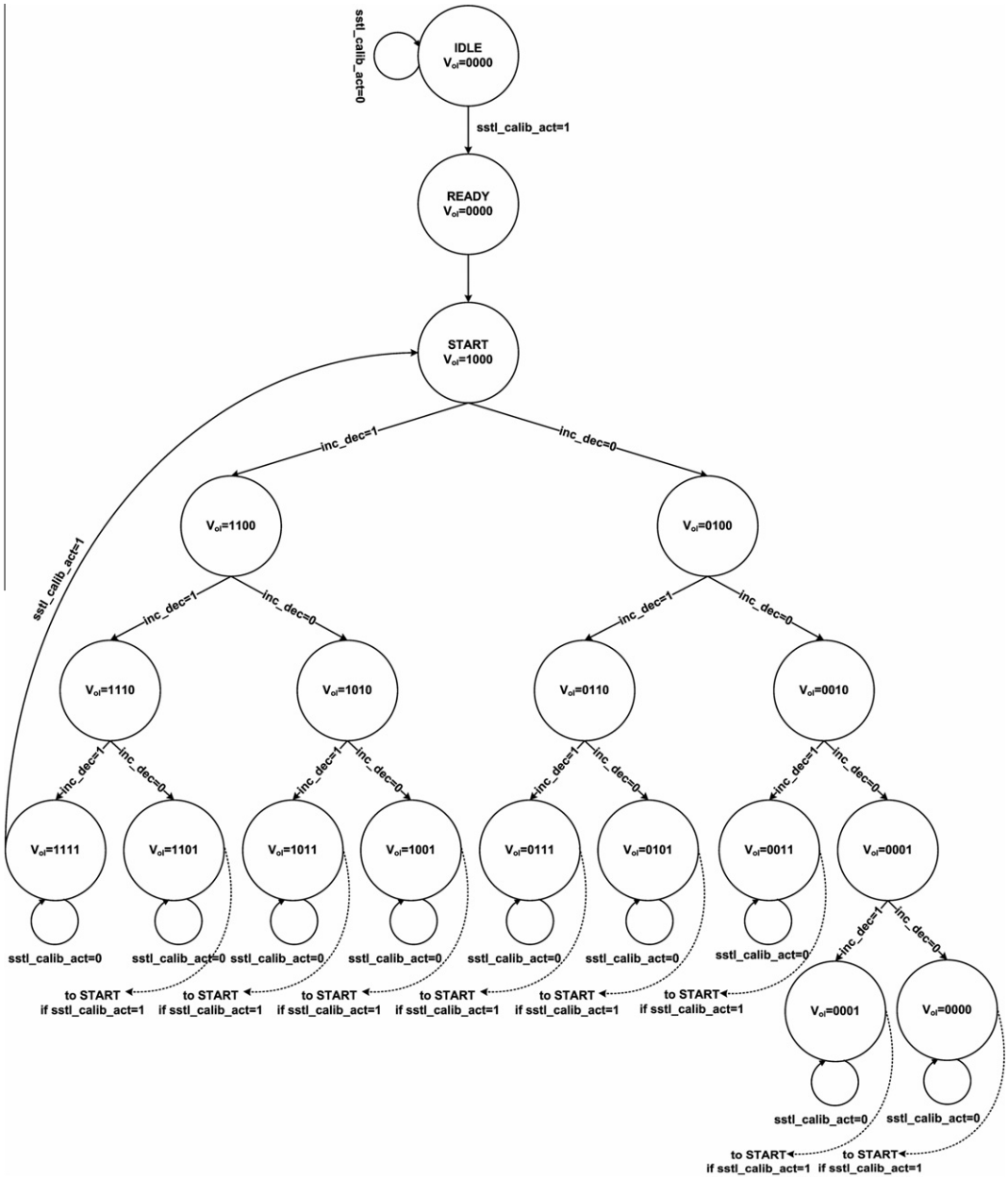

Fig. 8. Diagram of the binary search algorithm (pdFSM).

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(*sstl_calib_act*) of the pdFSM being the actual 'calibration activation' signal and the *calib_done* output of the pull-up FSM (puFSM) serving as the actual 'calibration done' signal. A functional description of the pdFSM is given in Fig. 8. Upon system reset, the pdFSM is at state IDLE which corresponds to *Vol* = 0000 and remains there until a pulse on the sstl_calib_act signal is received. After activation, it jumps to the READY state which is followed by the first state (START, *Vol* = 1000) of the pull-down binary search algorithm. At each following rising edge of the clock, the pdFSM samples the output of the comparator (the respective input of the pdFSM being *inc_dec*) and branches to the proper next value of the *Vol* bus, namely the next pdFSM state. These successive jumps form an approximation path through the algorithm tree and continue until the state machine reaches the final *Vol* binary setting. This value is the current optimum configuration for the pull-down resistor

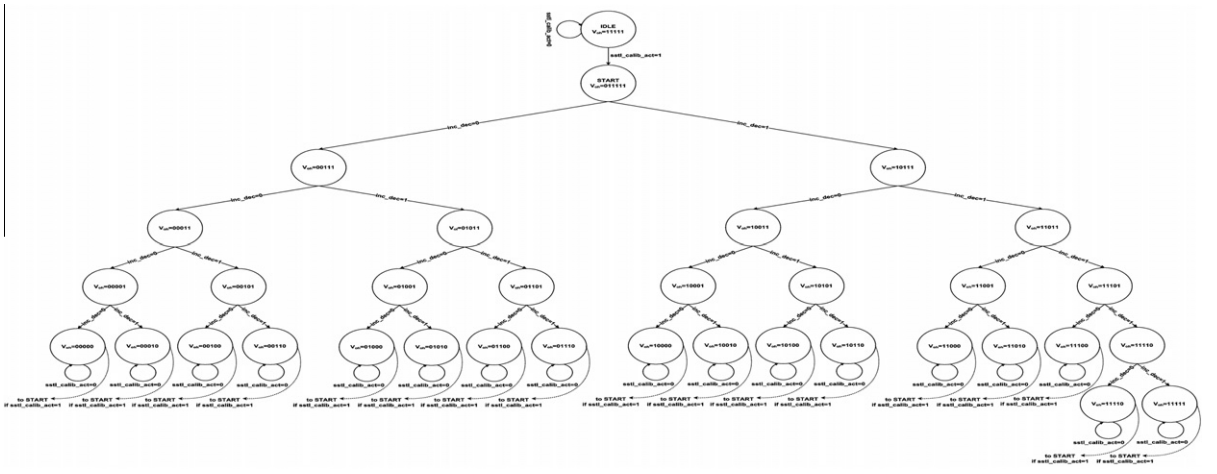

Fig. 9. Diagram of the binary search algorithm (puFSM).

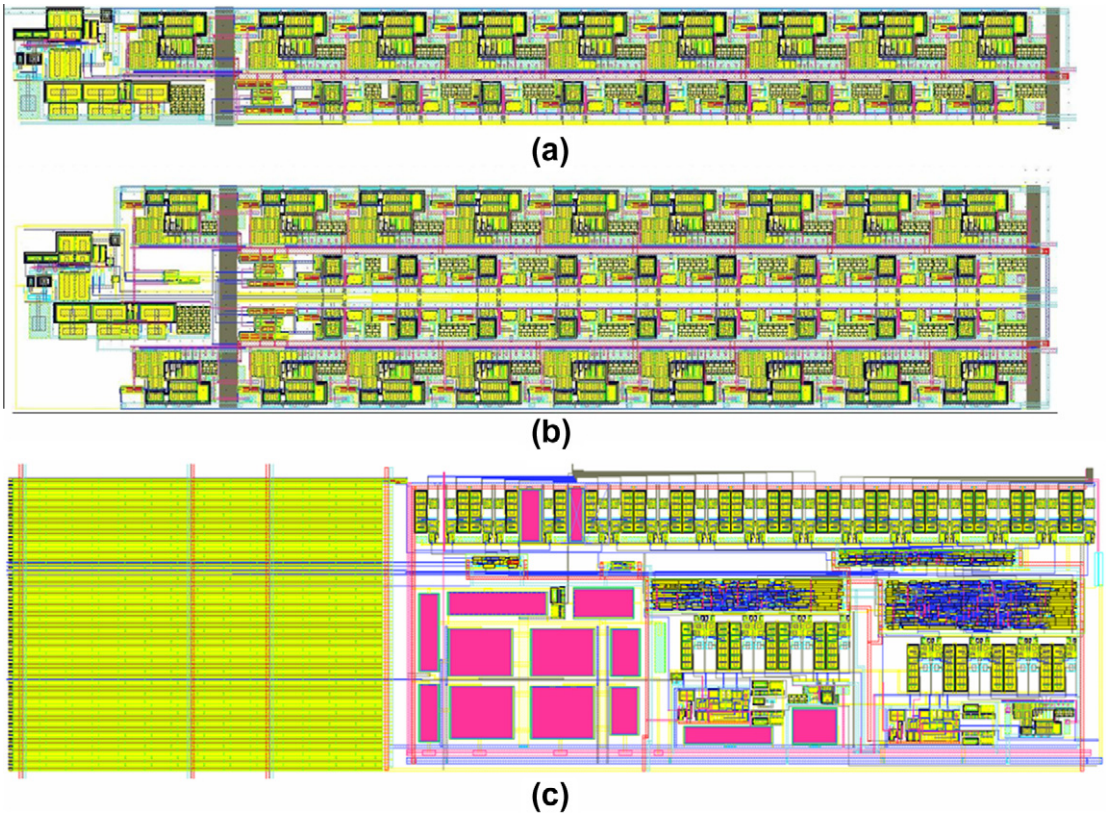

Fig. 10. The layout of the proposed single ended SSTL (a), the differential SSTL (b), and the calibration mechanism (c).

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network of the SSTL. When the pdFSM reaches its final state, the *calib_done* flag is asserted to indicate that the pull-down resistor network has been calibrated. The *calib_done* signal of the pdFSM is fed to the *sstl_calib_act* input of the puFSM so that the latter is activated after the former has completed its operation. The flag remains high until a reset is applied, or another request for re-calibration (another pulse on the *sstl_calib_act* signal) is registered, in which case the pdFSM jumps back to the START state.

A similar rationale applies to the pull-up FSM (Fig. 9). Clearly, the pull-up and pull-down algorithms are complementary to each other, as is the design of the resistor networks.

It should be noted that both FSMs operate using a clock frequency that is a sub multiple of the system clock frequency, i.e. the clock signal fed to the FSMs is the system clock divided by 2 (in the case that the system clock has a frequency between 200 and 400 MHz) or by 4 (in the case that the system clock has a frequency of 533 MHz). This gives adequate time margin for the stabilization of the clocked comparator decision and eliminates the need for a majority filter at its output. The final optimal *Voh* and *Vol* binary values are stored into a register file so that they remain stable and available to all SSTL IOs until they are updated by the next re-calibration procedure.

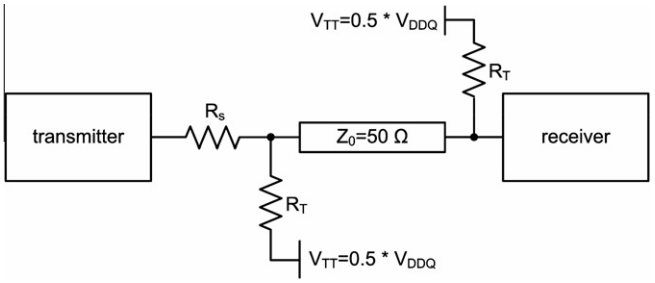

Fig. 11. Description of the testbench employed for the transient simulations.

Table 1
Experimental results for the pull-up and pull-down leg resistance.

PVT variation	Pull-up			Pull-down		
	150	240	300	150	240	300
27 °C/1.8 V or 1.5 V (TC)	151.0	241.2	309	145.7	240.6	307
100 °C/1.7 V or 1.4 V (TC)	151.4	240.0	306	152.4	237.9	301
0 °C/1.9 V or 1.6 V (TC)	151.5	241.8	310	149.0	234.0	290
27 °C/1.8 V or 1.5 V (BC)	146.1	235.3	292	144.7	238.7	295
100 °C/1.7 V or 1.4 V (BC)	146.4	235.6	293	152.0	237.5	289
0 °C/1.9 V or 1.6 V (BC)	145.8	234.0	290	143.0	231.2	263
27 °C/1.8 V or 1.5 V (WC)	159.8	248.2	340	146.0	242.5	335
100 °C/1.7 V or 1.4 V(WC)	165.9	250.1	350	159.2	246.1	340
0 °C/1.9 V or 1.6 V(WC)	163.1	249.1	341	148.0	243.9	344

TC: typical case, BC: Best case, WC: worst case.

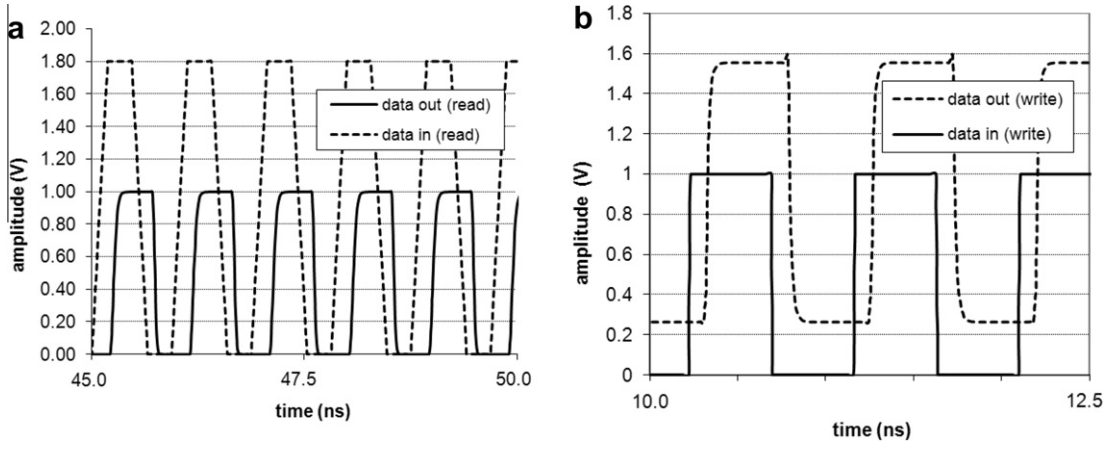

Fig. 12. Simulated waveforms for DDR2 read (a) and write (b) operations.

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In general, the time complexity of the presented calibration algorithms is O(N − 1), where N is the number of calibration bits at the output (Voh, Vol). Thus, the number of clock cycles required for the calibration closely follows the number of output calibration bits. In the case that N is large, the time complexity becomes almost O(N). The space complexity of the algorithms follow a $(2^N - 1)$ relation which exhibits a significant increase of the number of FSM states with the increase of N. However, since the FSMs operate at a sub-multiple of the system frequency, there is no need for fast one-hot state encoding which generally leads to larger synthesized designs. Instead, a simple state encoding scheme (such as binary or Binary Coded Decimal, BCD) can be employed in order to limit the size of FSMs synthesized for large values of N.

The resistance of the n- and p-leg can be calibrated at either VDDQ/VSSQ or at a midpoint voltage VDDQ/2. For the p-leg the resistance remains within the nominal ±3 Ohm spec when calculated at either the rails (VDDQ/VSS) or at VDDQ/2. For the n-leg the voltage comparison level should be lowered to VDDQ/4 when the resistance is calculated at VDDQ/VSS. In this case the resistor R_{ZQ} is placed between the ZQ_1 pin and VDDQ/2.

It has been derived through simulation experiments that the extra 300 Ohm couple of p- and n-type legs can be calibrated using the shifted (to the right by 2 bits) values of the *Voh* and *Vol* signals, respectively. Thus, two shift registers have been employed in the impedance calibration scheme.

Finally, the driving strength, determined by the output impedance, is dynamically calibrated through the dummy I/O buffers without affecting the operation of the main driver.

3. Performance summary

The main objective of the physical design was to verify the functionality of the circuit and the validity of the proposed architecture. For this purpose the choice of a 90 nm CMOS technology was judged to be adequate.

Fig. 10 shows the layout of the single ended SSTL (a), the differential SSTL (b) and the calibration mechanism (c). The die sizes are 45 × 350, 90 × 350, and 120 × 350 mm^2, respectively with a large amount of decoupling capacitors built into. It should be noticed that the calibration mechanism is capable of driving up to 12 SSTL drivers.

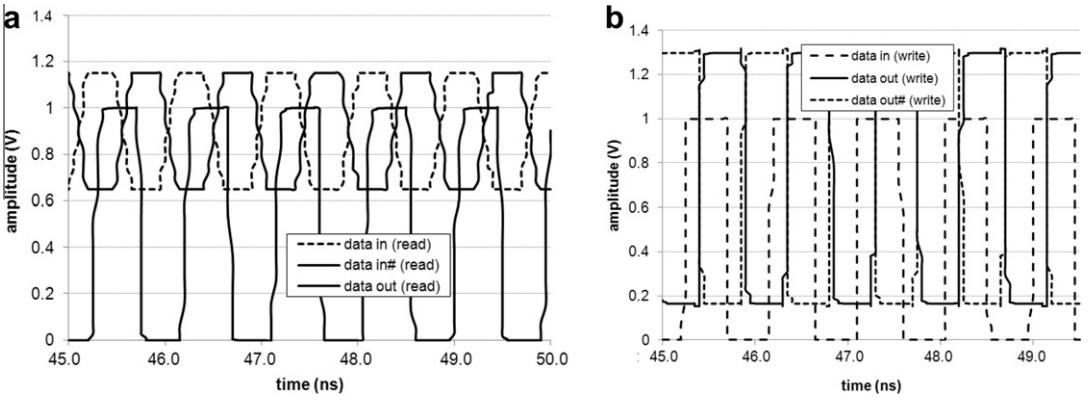

Fig. 13. Simulated waveforms for DDR3 read (a) and write (b) operations.

Table 2
Experimental ac and dc input/output signal values (DRR2 operation).

	Typical case 27 °C/1.8 V	Best case 0 °C/1.9 V	Worst case 100 °C/1.7 V	Specification[a,b]	Comments
V_{IH}(ac)	Test conditions			V_{REF} + 0.250	ac input logic high (minimum)
V_{IL}(ac)	Test conditions			V_{REF} − 0.250	ac input logic low (maximum)
I_{OH}(dc)	−14.5 mA	−15.02 mA	−13.46 mA	−13.4 mA	output minimum source dc current
I_{OL}(dc)	14.9 mA	15.15 mA	13.86 mA	13.4 mA	output minimum sink dc current
V_{OH}(ac)	1.59 V	1.63 V	1.55 V	V_{TT} + 0.603	min. required output pull-up under ac test
V_{OL}(ac)	226 mV	268 mV	225 mV	V_{TT} − 0.603	max. required output pull-down under ac test
R_{ON_PU}	18.875 Ohm	18.225 Ohm	20.738 Ohm	18 ± 3 Ohm	Pull-up output resistance
R_{ON_PD}	18.21 Ohm	17.875 Ohm	19.9 Ohm	18 ± 3 Ohm	Pull-down output resistance
Rtt(75)	74.151 Ohm	72.193 Ohm	81.240 Ohm	75 ± 20%	Effective impedance value (ODT, 75Ω)
Rtt(150)	154.5 Ohm	145.0 Ohm	175.0 Ohm	150 ± 20%	Effective impedance value (ODT, 150Ω)
Rtt(50)	50.1 Ohm	48.2 Ohm	60.2 Ohm	50 ± 20%	Effective impedance value (ODT, 50Ω)

[a] JEDEC standard No. 8-15A [15].
[b] JEDEC standard No. 79-2F [16], $V_{TT} = V_{REF} = 0.5 \cdot V_{DDQ}$.

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Table 3
Experimental ac and dc input/output signal values (DRR3 operation).

	Typical case 27 °C/1.5 V	Best case 0 °C/1.6 V	Worst case 100 °C/1.4 V	Specification[a]	Comments
V_{IH}(ac)	Test conditions			V_{REF} + 0.175	ac input logic high (minimum)
V_{IL}(ac)	Test conditions			V_{REF} − 0.175	ac input logic low (maximum)
V_{OH}(ac)	1.21 V	1.29 V	1.14 V	$V_{TT} + 0.1 \cdot V_{DDQ}$	AC output high measurement level
V_{OL}(ac)	297 mV	308 mV	246 mV	$V_{TT} - 0.1 \cdot V_{DDQ}$	AC output low measurement level
V_{IX}(ac)	55 mV	38 mV	68 mV	−150–150 mV	Differential input cross point voltage relative to VDD/2
R_{ON34Pd}	34.371 Ohm	33.029 Ohm	35.157 Ohm	34.3 ± 10%	Output driver impedance (pull-down)
R_{ON34Pu}	34.457 Ohm	33.429 Ohm	35.729 Ohm	34.3 ± 10%	Output driver impedance (pull-up)
$R_{TT120Pd240}$	240.6 Ohm	231.2 Ohm	246.1 Ohm	240 ± 10%	On-die termination effective resistance (pull-down)
$R_{TT120Pu240}$	241.2 Ohm	234.0 Ohm	250.1 Ohm	240 ± 10%	On-die termination effective resistance (pull-up)
$R_{TT60Pd120}$	120.3 Ohm	115.6 Ohm	123.1 Ohm	120 ± 10%	On-die termination effective resistance (pull-down)
$R_{TT60Pu120}$	120.6 Ohm	117.0 Ohm	125.1 Ohm	120 ± 10%	On-die termination effective resistance (pull-up)
$R_{TT40Pd80}$	80.2 Ohm	77.1 Ohm	82.0 Ohm	80 ± 10%	On-die termination effective resistance (pull-down)
$R_{TT40Pu80}$	80.4 Ohm	78.0 Ohm	83.4 Ohm	80 ± 10%	On-die termination effective resistance (pull-up)
$R_{TT30Pd60}$	60.2 Ohm	57.8 Ohm	61.5 Ohm	60 ± 10%	On-die termination effective resistance (pull-down)
$R_{TT30Pu60}$	60.3 Ohm	58.5 Ohm	62.5 Ohm	60 ± 10%	On-die termination effective resistance (pull-up)
$R_{TT20Pd40}$	40.1 Ohm	38.5 Ohm	41.0 Ohm	40 ± 10%	On-die termination effective resistance (pull-down)
$R_{TT20Pu40}$	40.2 Ohm	39.0 Ohm	41.7 Ohm	40 ± 10%	On-die termination effective resistance (pull-up)

[a] JEDEC standard No. 79-3E [17].

Extensive transient simulations have been carried out using the Cadence® Virtuoso® Spectre® circuit simulator and the testbench shown in Fig. 11. Spectre® is tightly integrated with the Virtuoso custom design platform and provides detailed and accurate transistor-level analysis for the mixed-signal circuit under study. On-DIMM resistor R_s is 20 Ohm in the DDR2 mode and 15 Ohm in the DDR3 mode of operation whereas R_T is 50 Ohm in both cases. One SSTL driver in transmitting mode (Transmitter) and one in receiving mode (Receiver) have been furthermore used in order to better represent an as realistic as possible scenario.

The resistance values of the 150/240/300 Ohm p- and n-leg as a function of the temperature, voltage supply and process variations are shown in Table 1. The supply voltage is varied from 1.7 to 1.9 V and the temperature from 0 °C to 100 °C. It is obvious that all required output and the termination resistances can be achieved using the appropriate combination of the eight available p- and n-legs or the extra 300 Ohm p- and n-leg. The resistance value of the merged driver (when operating as termination driver) has been also simulated and can be controlled to be 150, 75 or 50 Ohm (DDR2) and 30, 40, 60 or 120 Ohm (DDR3).

The experimental results for the calibrated operation of the input and the output buffer for DDR2 and DDR3 operation are shown in Figs. 12 and 13 respectively. By employing a transmission gate to form the combo SSTL I/O the maximum operating frequency is limited to 1.15 GHz thus meeting the DDR2/3 requirements. The same driver, without the transmission gate, operates up to 1.32 GHz.

The slew rate can be controlled from 0.5 to 15 V/ns for a 4-pF load using the control signals UpSlew and DnSlew. The UpSlew signal is generated by using a voltage divider formed by a 1 kOhm internal resistor connected to VDDQ (a dedicated power supply pin could be used to reduce the Simultaneous Switching Output-SSO effect) and a variable external resistor which should be connected to VSS. DnSlew is generated by using a voltage divider formed by a 1 kOhm internal resistor connected to VSS (a dedicated ground pin could be used to reduce the SSO effect) and a variable external resistor which should be connected to VDDQ.

In Tables 2 and 3, the experimental ac and dc input/output signal values for the DDR2 and the DRR3 operation modes are presented together with the operating parameters defined by the corresponding standard. The results drawn by these Tables lead to the conclusion that our design does meet the requirements.

4. Conclusion

In this paper, a 1 GHz DDR2/3 combo SSTL driver achieving all DDR2 and DDR3 operations, and incorporating all relevant (DDR2/3) JEDEC features has been presented. Having the design been optimized for area-a small die area of 0.032 mm^2 is required- and performance-characteristics, it is furthermore equipped with all necessary functionality for ensuring signal integrity and reduced output skew, including efficient mechanisms for supporting slew rate control and impedance control mechanisms through ODT and OCD calibration, whereas for the latter one the option of calibration not only at the rails (VDDQ/VSS) but also at VDDQ/2 is provided. Experimental results, drawn by the implementation of this device in 90 nm CMOS process (TSMC) have demonstrated its robustness across PVTs and high performance in all modes of operation at a speed of at least 1 GHz. This DDR2/3 combo SSTL driver to our knowledge, is the first implementation presented in the literature and is expected to be widely used in high-performance memory PHYs and devices of the future, facilitating the transition from designs currently employing DDR2 interfaces to DDR3 ones.

Please cite this article in press as: Plessas F et al. A 1 GHz, DDR2/3 SSTL driver with On-Die Termination, strength calibration, and slew rate control. Comput Electr Eng (2012), doi:10.1016/j.compeleceng.2011.12.012

References

[1] Guha R, Bagherzadeh N, Chou P. Resource management and task partitioning and scheduling on a run-time reconfigurable embedded system. Comp Elect Eng 2009;35:258–85.
[2] Chen N, Lin H. Investigation of Low Cost Consumer Electronic System Using 1066-Mb/s DDR2 Interface Design, In: Proc. 9th International Conference on Solid-State and Integrated-Circuit Technology, ICSICT 2008. China: Beijing; 2008. p. 1203–1206.
[3] Farrell T. Core Architecture Doubles MEM Data Rate, Electronic Engineering Times Asia (2005). Available from: <http://www.eetasia.com/ARTICLES/2005DEC/B/EEOL_2005DEC16_STOR_TA.pdf>.
[4] Yoo C, Kyung KH, Lim K, Lee HC, Chai JW, Heo NW, et al. A 1.8V 700-Mb/s/pin 512-Mb DDR-II SDRAM With On-Die Termination and Off-Chip Driver Calibration. IEEE J Solid-State Circuits 2004;39:941–51.
[5] Matano T, Takai Y, Takahashi T, Sakito Y, Takaishi Y, Fujisawa H, Kubouchi S, Narui S, Arai K, Morino M, Nakamura M, Miyatake S, Sekiguchi T, Koyama K, Miyazawa K. A 1-Gb/s/pin 512-Mb DDRII SDRAM Using a Digital DLL and a Slew-Rate-Controlled Output Buffer, In: Proc. Symposium on VLSI Circuits, Digest of Technical Papers, VLSIC 2002, Honolulu, Hawaii, USA; 2002. p. 112–113.
[6] Fujisawa H, Nakamura M, Takai Y, Koshikawa Y, Matano T, Narui S, et al. 1.8-V 800-Mb/s/pin DDR2 and 2.5-V 400-Mb/s/pin DDR1 Compatibly Designed 1-Gb SDRAM With Dual-Clock Input-Latch Scheme and Hybrid Multi-Oxide Output Buffer. IEEE J Solid-State Circuits 2005;40:862–9.
[7] Park C, Chung H, Lee YS, Kim J, Lee J, Chae MS, et al. A 512-Mb DDR3 SDRAM Prototype With C_{IO} Minimization and Self-Calibration Techniques. IEEE J Solid-State Circuits 2006;41:831–8.
[8] Esch Jr. G, Chen T. Design of CMOS IO Drivers with Less Sensitivity to Process, Voltage, and Temperature Variations, In: Proc. Second IEEE International Workshop on Electronic Design, Test and Applications, DELTA 2004, Perth, Australia; 2004. p. 312–317.
[9] Sohn YS, Bae SJ, Park HJ, Cho SI. A 1.2Gbps CMOS DFE Receiver with the Extended Sampling Time Window for Application to the SSTL Channel, In: Proc. Symposium on VLSI Circuits, Digest of Technical Papers, VLSIC 2002, Honolulu, Hawaii, USA; 2002. p. 92–93.
[10] Kim NS, Yoon YJ, Cho UR, Byun HG. Programmable and Automatically Adjustable On-Die Terminator for DDR3-SRAM Interface, In: Proc. IEEE 2003 Custom Integrated Circuits Conference, CICC 2003, San Jose, CA, USA; 2003. p. 391–394.
[11] Cho UR, Kim TH, Yoon YJ, Lee JC, Bae DG, Kim NS, et al. A 1.2-V 1.5-Gb/s 72-Mb DDR3 SRAM. IEEE J Solid-State Circuits 2003;38:1943–51.
[12] Konstadinidis G, Normoyle K, Wong S, Bhutani S, Stuimer H, Johnson T, et al. Implementation of a Third-Generation 1.1-GHz 64-bit Microprocessor. IEEE J Solid-State Circuits 2002;37:1461–9.
[13] Alexandropoulos A, Davrazos E, Plessas F, Birbas M. A novel 1.8 V, 1066 Mbps, DDR2, DFI-compatible, Memory Interface, In: Proc. 2010 IEEE Annual Symposium on VLSI, ISVLSI '10, Kefalonia, Greece; 2010. p. 387–392.
[14] <http://www.synopsys.com/dw/ipdir.php?ds=dwc_ddr_multiphy>, accessed Dec. 29, 2011.
[15] JEDEC Standard, Stub Series Terminated Logic for 1.8V (SSTL_18), JESD8-15A (Revision of JESD8-15), JEDEC Solid State Technology Association, September, 2003.
[16] JEDEC Standard, DDR2 SDRAM Specification, JESD79-2F (Revision of JESD79-2E), JEDEC Solid State Technology Association, November, 2009.
[17] JEDEC Standard, DDR3 SDRAM Specification, JESD79-3E (Revision of JESD79-3D), JEDEC Solid State Technology Association, July, 2010.
[18] Chen CK, Guo WD, Yu CH, Wu RB. Signal integrity analysis of DDR3 high-speed memory module, In: Proc. Electrical Design of Advanced Packaging and Systems Symposium, EDAPS 2008, Seoul, Korea; 2008. p. 101–104.
[19] Wirick A, Ulrich S, Pham N, Cases M, de Araujo DN. Design and modeling challenges for DDR II memory subsystems, In: Proc. Electrical Performance of Electronic Packaging, EPEPS 2003, Princeton, NJ, USA; 2003. p. 229–232.
[20] Dally WJ, Poulton WJ. Digital systems engineering. Cambridge UK: Cambridge University Press; 1998.
[21] Keeth B, Baker RJ, Johnson B, Lin F. DRAM circuit design. New Jersey: Wiley; 2008.
[22] Baker RJ. CMOS circuit design, layout and simulation. New Jersey: Wiley; 2008.

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Please cite this article in press as: Plessas F et al. A 1 GHz, DDR2/3 SSTL driver with On-Die Termination, strength calibration, and slew rate control. Comput Electr Eng (2012), doi:10.1016/j.compeleceng.2011.12.012