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A sub-1V supply CMOS voltage reference generator

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SUMMARY

An integrated sub-1V voltage reference generator, designed in standard 90-nm CMOS technology, is presented in this paper. The proposed voltage reference circuit consists of a conventional bandgap core based on the use of p-n-p substrate vertical bipolar devices and a voltage-to-current converter. The former produces a current with a positive temperature coefficient (TC), whereas the latter translates the emitter-base voltage of the core p-n-p bipolar device to a current with a negative TC. The circuit includes two operational amplifiers with a rail-to-rail output stage for enabling stable and robust operation overall process and supply voltage variations while it employs a total resistance of less than 600 KΩ. Detailed analysis is presented to demonstrate that the proposed circuit technique enables die area reduction. The presented voltage reference generator exhibits a PSRR of 52.78 dB and a TC of 23.66 ppm/°C in the range of −40 and 125°C at the typical corner case at 1 V. The output reference voltage of 510 mV achieves a total absolute variation of ±3.3% overall process and supply voltage variations and a total standard deviation, σ, of 4.5 mV, respectively, in the temperature range of −36 and 125°C. Copyright © 2011 John Wiley & Sons, Ltd.

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KEY WORDS: low power; sub-1V operation; bandgap reference; temperature stability; temperature range; temperature coefficient (TC); Power Supply Rejection Ratio (PSRR); weak inversion; robustness

1. INTRODUCTION

Reference voltage generators provide a stable reference voltage over process, supply voltage and temperature variations. The design of a conventional bandgap voltage reference (BGR) gives a very stable output voltage, fulfilling the aforementioned requirements, since it is nearly equal to the bandgap of silicon (1.22 V). However, for sub-1V design, the traditional BGR design method cannot be applied [1]. As CMOS technology scales down the demand for low supply voltage sub-bandgap circuits with structure size reduction [2] raises drastically. Today's available standard CMOS technologies at 90 nm or below provide MOSFET devices with low threshold voltage and substrate vertical p-n-p bipolar transistors which are accurately modeled, thus low supply voltage design is facilitated. Banba *et al.* proposed a BGR circuit [3] capable of operating at sub-1V supply voltage with a very stable output reference voltage, which was proven to be a key concept for sub-1V CMOS voltage reference circuit designs.

In the past, nonstandard CMOS process options have been proposed [3–5] (native transistors, DTMOST, BiCMOS) for low supply voltage reference generators design, yet the implementation

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of these circuits requires specialized modeling and characterization as well as extra mask layers, and process steps that increase the cost. Moreover, the reproducibility and the portability of the design are poor when employing these design approaches. On the other hand, operation of MOSFET devices in the subthreshold regime allows for power dissipation reduction while also more efficient use of the available headroom is employed, thus operation at sub-1V supply voltage becomes feasible. In [6–10], MOSFET devices are biased in weak inversion in a variety of circuits' configurations such that PTAT and CTAT signals are generated via their gate-source voltage targeting at a stable reference voltage over temperature. In addition to the above mentioned [3–10], several other voltage reference generators [11–21] have been reported in the past, which however due to their limited temperature range of operation, limited stability and requirement for large area or for higher than 0.9 V minimum supply voltage are not fully suitable for sub-1V, wide temperature range applications where the supply voltage varies between 0.9 V and higher than 1 V voltages.

The prime objective of this work is to develop a voltage reference generator of sub-1V supply voltage with low power consumption and relatively small die area. The output reference absolute voltage deviation should be limited around 6% overall process and supply voltage variations (0.9–1.1 V) in the wide temperature range of -40 to 125°C. This reference circuit should also provide a proportional to absolute temperature (PTAT) current to other sub-circuits where temperature compensation techniques are necessary.

The proposed voltage reference circuit consists of a conventional bandgap core, where a PTAT current flows, and a voltage-to-current (V-to-I) converter that transforms the complementary to absolute temperature (CTAT) emitter-base voltage of the core bipolar device to a current with negative temperature coefficient (TC). The two currents are properly copied and added producing a very stable current with low temperature and supply voltage dependency which in turn is linearly transformed into a constant output reference voltage via a resistance. The use of the V-to-I converter replaces one of the two equal, large resistors R1, R3 in the classical sub-1V voltage reference of Banba *et al.* (Figure 1) and reduces the value of the resistor R1 (or R3) required for the generation of the CTAT current without sacrificing the circuit performance. The latter is proven through a detailed circuit analysis. Therefore, die area reduction is achieved, where the level of the area saved depends on the V-to-I converter implementation and thus its die area.

This paper is organized as follows. In Section 2, we discuss the proposed sub-1V voltage reference generator topology, the V-to-I converter and start-up circuit realization and we explain

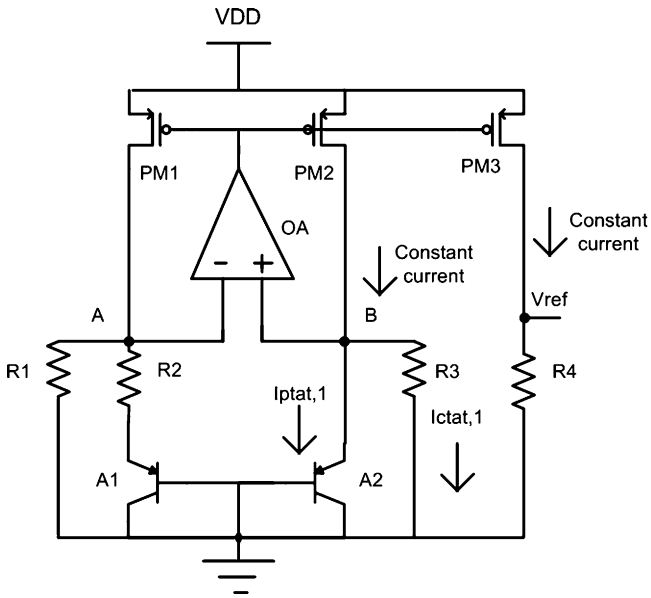

Figure 1. Sub-1V supply CMOS voltage reference generator proposed by Banba *et al.* [2].

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various design trade-offs. The simulation results are also given. In addition, the necessary circuit analysis is presented in order to demonstrate the level of the area reduction that is achieved by applying the proposed circuit technique. In Section 3, we describe the overall implementation together with the post-layout simulation results followed by a comparison with previously published work. Finally, we provide our conclusions in Section 4.

2. CIRCUIT DESIGN

It is well known that the emitter-base voltage of p-n-p bipolar junction substrate transistors that are available in CMOS processes shows limited linearity in a very wide temperature range with the result that curvature compensation is required for high precision applications. Nevertheless, by using MOSFET devices in weak inversion [6–10] such that the threshold voltage temperature dependence is employed for gate-source CTAT voltages generation did not lead to a purely linear voltage function with respect to temperature. The latter is demonstrated in [8]. Moreover, as it is reported in [11], the assumption that the threshold voltage is a linear function of temperature may hold approximately in the temperature range between -20 and 120°C. Furthermore, the fact that the subthreshold slope n is a temperature-dependent parameter may also result in the aforementioned nonlinearity as it is reported in [7]. As a result, the use of p-n-p bipolar junction substrate transistors still remains a very good option for the design of an accurate voltage reference generator circuit.

In [10], a nanowatt BGR with 0.5 V supply voltage has been designed, which uses the temperature characteristics of PMOSFETs and NMOSFETs devices but suffers from poor PSRR (Power Supply Rejection Ratio) performance (14 dB). In [12], weak inversion regime is employed to overcome the bottleneck caused by the devices threshold voltage while the PTAT and CTAT signals are produced by using substrate vertical p-n-p bipolar junction transistors. In [13], a CMOS voltage reference circuit is reported that exploits the temperature dependence of NMOS and PMOS threshold voltages to form temperature insensitive reference voltage, yet an issue of concern in this design approach is that the reference voltage depends on process parameters that may result in strong fluctuations over process variations [14]. Another design method for a BGR is reported in [11] where a MOSFET device is biased at the ZTC (zero temperature coefficient) point via an external current source. The latter exploits the mutual compensation of MOSFET mobility and threshold voltage temperature variations and ideally leads to a temperature insensitive reference voltage under the conditions that the mobility temperature drift is proportional to T^{-2} and the threshold voltage varies linearly with temperature. However, the mobility temperature dependence may be different than T^{-2} since it is a process-dependent parameter that deteriorates the temperature stability of a current or voltage reference circuit in which the ZTC method is applied. Other authors had expressed their doubts [15] on the reproducibility of ZTC reference circuits. A 1 V CMOS bandgap based on resistive subdivision is reported in [16] yet this technique was proven to be insufficient for precision voltage reference circuits operating in a wide temperature range due to the increase in the curvature error. Moreover, in the latter technique the total resistance of the circuit resistors exceeds 1 MΩ. In [20, 21], sub-1V accurate BGR circuits are reported with very good performance in the range of -40 to 125°C, nevertheless their die area is not positioned among the lowest reported in the literature. In the latter, the reverse bandgap principle is employed, which was initially proposed by R. Widlar in 1978.

The proposed voltage reference generator circuit is depicted in Figure 2. The substrate vertical bipolar devices B1, B2 have an emitter area ratio of 1:8. The difference in their emitter-base voltages is applied across the resistance R1 due to the presence of the operational amplifier OA1 that controls the PMOS devices PM1, PM2 such that the voltages at nodes A, B are equal. As a result, the current that flows via PM1 and PM2 is of PTAT type. This PTAT-type current is used to bias both the operational amplifiers OA1 and OA2 via the devices PM6, NM1, NM2 and NM3. The components OA2, PM3 and R2 form a V-to-I converter [22], V–I that transforms the CTAT emitter-base voltage of B2 into a CTAT current which flows via the PMOS device PM3 and

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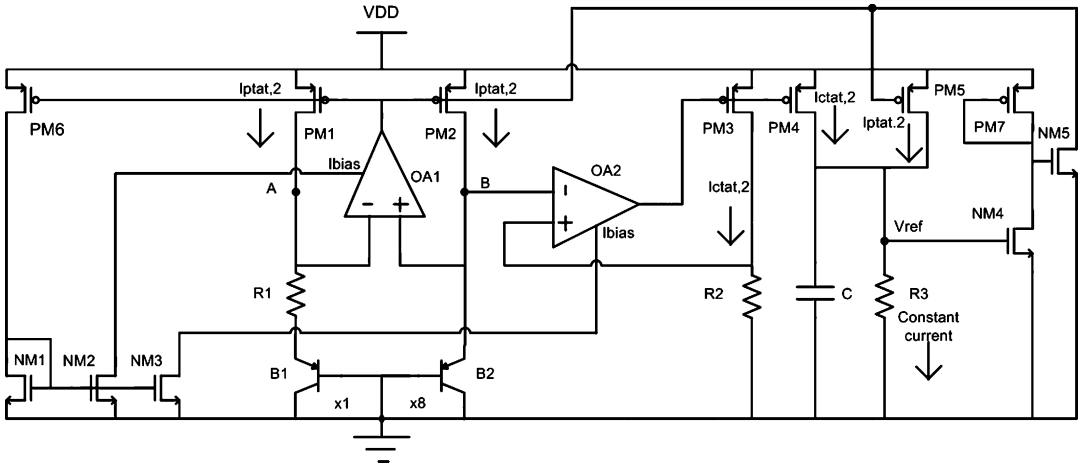

Figure 2. The proposed sub-1V supply CMOS voltage reference generator design.

resistance R2. The CTAT current flowing via PM3 is appropriately copied to PM4, whereas the PTAT current flowing via PM1, PM2 is similarly copied to PM5. Subsequently, when these two copied currents with opposite temperature dependencies are added together a constant strongly temperature independent current is produced. The latter is then linearly transformed into an ideally temperature independent voltage via the resistance R3. It should be noted that the CTAT current generation via the V–I converter guarantees robust operation of the proposed circuit over supply voltage, process and temperature variations. The output reference voltage of the proposed circuit is given by Equation (1) under the assumption that $R2 = R_{\mathrm{CTAT},2}$ and $R1 = R_{\mathrm{PTAT},2}$

$$V_{\mathrm{ref}} = R3 \cdot \left(\frac{\Delta V_{\mathrm{EB(B1,B2)}}}{R_{\mathrm{PTAT},2}} + \frac{V_{\mathrm{EB(B2)}}}{R_{\mathrm{CTAT},2}} \right) \tag{1}$$

$\Delta V_{\mathrm{EB(B1,B2)}}$ represents the voltage difference between the emitter-base voltages of B1, B2, whereas $V_{\mathrm{EB(B2)}}$ represents the emitter-base voltage of B2. As it can be seen from Equation (1), the temperature dependencies of $R_{\mathrm{PTAT},2}$ and $R_{\mathrm{CTAT},2}$ are cancelled by that of R3. The output reference voltage is ideally independent of temperature variations if the slope $\mathrm{d}V_{ref}/\mathrm{d}T$ equals zero, thus by differentiating both sides of Equation (1) the following equation can be derived:

$$\frac{\mathrm{d}\Delta V_{\mathrm{EB(B1,B2)}}}{\mathrm{d}T} \Big/ \frac{\mathrm{d}V_{\mathrm{EB(B2)}}}{\mathrm{d}T} = \frac{R_{\mathrm{PTAT},2}}{R_{\mathrm{CTAT},2}} \tag{2}$$

where $\mathrm{d}\Delta V_{\mathrm{EB(B1,B2)}}/\mathrm{d}T$, $\mathrm{d}V_{\mathrm{EB(B2)}}/\mathrm{d}T$ are the slopes of the voltages $\Delta V_{\mathrm{EB(B1,B2)}}$ (PTAT) and $V_{\mathrm{EB(B2)}}$ (CTAT), respectively, in the proposed circuit of Figure 2 at a specific temperature T_0.

The proposed voltage reference generator topology relies on the proper replicas of the PTAT and CTAT currents that are generated by the conventional bandgap core (B1, B2, PM1, PM2, OA1, R1) and the V–I converter (OA2, PM3, R2), respectively. This implies that the need for very large output impedance of devices PM1–PM5 is crucial. However, there is not much available headroom for using cascode current sources. In order to compensate for this problem the bias current of devices PM1, PM2 was selected to be low (on the order of μAs) and a large MOSFET length was used. This provides them with high output impedance on the order of MΩ. The resistance R1 was thus set equal to a few tenths of KΩ for achieving a low current via B1, B2. The length of devices PM5 and PM6 can be chosen to be on the order of few μms as well. Similarly, the bias current of PM3 was also set to be very small.

If we assume that the current I of devices PM1–PM5 in Figure 2 is equal to the current of devices PM1–PM3 in Figure 1, and that devices PM1–PM5 in Figure 2 are identical to devices PM1–PM3 in Figure 1, then the devices PM1–PM3 in Figure 1 and PM1–PM5 in Figure 2 have the same output impedance. This implies that these devices suffer from the same copy current

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error. Consequently, the voltage error due to the copy current error in the output reference voltage of both circuits of Figure 1, Figure 2 is the same for a load resistance R3 in Figure 2 equal to the half the load resistance R4 in Figure 1 or equivalently for the same output reference voltage level. It is also assumed that the device A1 is identical to B1 and A2 is identical to B2 in Figure 1 and 2. For the classic circuit of Figure 1 it holds

$$I = I_{\mathrm{PTAT},1} + I_{\mathrm{CTAT},1} \tag{3}$$

For the circuit of Figure 1, let $R1 = R3 = R_{\mathrm{CTAT},1}$ and $R2 = R_{\mathrm{PTAT},1}$. Equation (3) can be written as follows:

$$I = \frac{\Delta V_{\mathrm{EB(A1,A2)}}}{R_{\mathrm{PTAT},1}} + \frac{V_{\mathrm{EB(A2)}}}{R_{\mathrm{CTAT},1}} \tag{4}$$

Similarly, by applying Equation (2) to the classic circuit of Figure 1, we have

$$\frac{\mathrm{d}\Delta V_{\mathrm{EB(A1,A2)}}}{\mathrm{d}T} \Big/ \frac{\mathrm{d}V_{\mathrm{EB(A2)}}}{\mathrm{d}T} = \frac{R_{\mathrm{PTAT},1}}{R_{\mathrm{CTAT},1}} \tag{5}$$

where $\mathrm{d}\Delta V_{\mathrm{EB(A1,A2)}}/\mathrm{d}T$, $\mathrm{d}V_{\mathrm{EB(A2)}}/\mathrm{d}T$ are the voltage slopes of voltages $\Delta V_{\mathrm{EB(A1,A2)}}$ and $V_{\mathrm{EB(A2)}}$, respectively, in the circuit of Figure 1 at a specific temperature T_0.

Equation (4) due to Equation (5) can be written as:

$$I = \frac{V_T \cdot \ln A}{\left(\frac{\mathrm{d}\Delta V_{\mathrm{EB(A1,A2)}}}{\mathrm{d}T} \Big/ \frac{\mathrm{d}V_{\mathrm{EB(A2)}}}{\mathrm{d}T}\right) \cdot R_{\mathrm{CTAT},1}} + \frac{V_{\mathrm{EB(A2)}}}{R_{\mathrm{CTAT},1}} \tag{6}$$

where V_T is the thermal voltage, A is the emitter area ratio of A1, A2 and B1, B2 in Figures 1 and 2, respectively.

Equation (6) can be written as follows:

$$R_{\mathrm{CTAT},1} = \frac{V_T \cdot \ln A}{\left(\frac{\mathrm{d}\Delta V_{\mathrm{EB(A1,A2)}}}{\mathrm{d}T} \Big/ \frac{\mathrm{d}V_{\mathrm{EB(A2)}}}{\mathrm{d}T}\right) \cdot I} + \frac{V_{\mathrm{EB(A2)}}}{I} \tag{7}$$

We also have:

$$R_{\mathrm{PTAT},2} = \frac{\Delta V_{\mathrm{EB(B1,B2)}}}{I_{\mathrm{PTAT},2}} = \frac{V_T \cdot \ln A}{I} \tag{8}$$

Equation (7) due to (8) can be written as:

$$R_{\mathrm{CTAT},1} = \frac{R_{\mathrm{PTAT},2}}{\left(\frac{\mathrm{d}\Delta V_{\mathrm{EB(A1,A2)}}}{\mathrm{d}T} \Big/ \frac{\mathrm{d}V_{\mathrm{EB(A2)}}}{\mathrm{d}T}\right)} + \frac{V_{\mathrm{EB(A2)}}}{I} \tag{9}$$

Using (2), Equation (9) becomes:

$$R_{\mathrm{CTAT},1} = \frac{\left(\frac{\mathrm{d}\Delta V_{\mathrm{EB(B1,B2)}}}{\mathrm{d}T} \Big/ \frac{\mathrm{d}V_{\mathrm{EB(B2)}}}{\mathrm{d}T}\right) \cdot R_{\mathrm{CTAT},2}}{\left(\frac{\mathrm{d}\Delta V_{\mathrm{EB(A1,A2)}}}{\mathrm{d}T} \Big/ \frac{\mathrm{d}V_{\mathrm{EB(A2)}}}{\mathrm{d}T}\right)} + \frac{V_{\mathrm{EB(A2)}}}{I} \tag{10}$$

Owing to the exponential dependence of the collector current of A2 on voltage $V_{\mathrm{EB(A2)}}$, small changes in the A2 collector current cause very small changes in $V_{\mathrm{EB(A2)}}$. Subsequently, for the simplification of the foregoing analysis and although the current flowing via A2 of the classic

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circuit (Figure 1) is smaller than the current flowing via B2 of the presented circuit (Figure 2) we can assume that:

$$V_{\mathrm{EB(A2)}} \cong V_{\mathrm{EB(B2)}} \tag{11a}$$

$$\frac{V_{\mathrm{EB(A2)}}}{I} \cong \frac{V_{\mathrm{EB(B2)}}}{I} = R_{\mathrm{CTAT},2} \tag{11b}$$

$$\frac{\mathrm{d}V_{\mathrm{EB(A2)}}}{\mathrm{d}T} \cong \frac{\mathrm{d}V_{\mathrm{EB(B2)}}}{\mathrm{d}T} \tag{11c}$$

As the devices A1, A2 in Figure 1 are identical to the devices B1, B2, respectively, in Figure 2 we get:

$$\Delta V_{\mathrm{EB(A1,A2)}} = \Delta V_{\mathrm{EB(B1,B2)}} = V_T \cdot \ln A \tag{12}$$

By differentiating Equation (12) with respect to temperature we derive:

$$\frac{\mathrm{d}\Delta V_{\mathrm{EB(A1,A2)}}}{\mathrm{d}T} = \frac{\mathrm{d}\Delta V_{\mathrm{EB(B1,B2)}}}{\mathrm{d}T} = \frac{dV_T(T)}{\mathrm{d}T} \cdot \ln A \tag{13}$$

Equation (10) due to Equations (11c) and (13) can be written as:

$$R_{\mathrm{CTAT},1} \cong 2 \cdot R_{\mathrm{CTAT},2} \tag{14}$$

Equation (14) proves that the proposed circuit (Figure 2) and the classic circuit (Figure 1) have the same voltage error due to the copy current error in their output reference voltage when the following condition is met: the resistance required for producing the CTAT-type current in the proposed circuit of Figure 2 is approximately half the corresponding resistance required in the classic circuit of Figure 1 under the assumption that the current that flows via PM1, PM2 in both circuits is numerically equal to I. Consequently, the circuit architecture proposed in this work saves die area which can be calculated by Equation (15)

$$\text{Area saving } (\%) = 100X \frac{(\text{Area})|_{\mathrm{OpAmp}} + (\text{Area})|R_{\mathrm{CTAT},2} - 2X(\text{Area})|R_{\mathrm{CTAT},1}}{2X(\text{Area})|R_{\mathrm{CTAT},1}} \tag{15}$$

The layout area of an integrated resistor, R, is given by:

$$\text{Area} = R \cdot \frac{S \cdot W}{\rho} \tag{16}$$

where R is the resistance value, ρ is the material specific resistance, S is the resistor cross-section and W is the resistor width. If the layout area of OA2 equals λ times the layout area of resistor $R_{\mathrm{CTAT},2}$ and if the resistors $R_{\mathrm{CTAT},1}$, $R_{\mathrm{CTAT},2}$ have the same cross-section and width and are made of the same material, then Equation (15) can be written due to (16) as:

$$\text{Area Saving}(\%) = 100X \frac{(\lambda+1) \cdot R_{\mathrm{CTAT},2} - 2 \cdot R_{\mathrm{CTAT},1}}{2 \cdot R_{\mathrm{CTAT},1}} \tag{17}$$

If it is assumed that the layout area of OA2 equals the layout area of the resistor $R_{\mathrm{CTAT},2} (\lambda = 1)$, then the use of the V-to-I converter V–I ensures that a layout area saving exists of about 50% due to Equations (14) and (17). This holds for the presented implementation. In the case that the layout area of OA2 can be neglected when compared with the layout area of the resistor $R_{\mathrm{CTAT},2} (\lambda \ll 1)$, and provided that OA2 is a single stage implementation, then the use of the V-to-I converter V–I ensures that a layout area saving exists of about 75% due to Equations (14) and (17). However, for enabling proper circuit operation at very low temperatures overall process corners, the operational amplifier design requires additional complexity, thus its corresponding die area increases.

As the output voltage of the voltage reference generator should be high enough for maintaining low percentage variation over process, supply voltage and temperature variations, the selected

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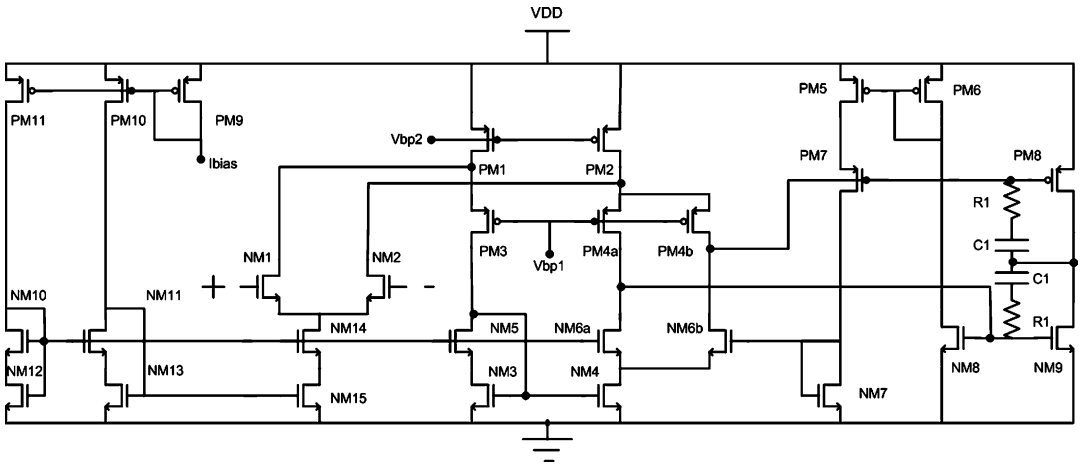

Figure 3. Operational amplifier design with rail-to-rail output stage (OP1/OP2).

value of 510 mV was proven to be adequate for an overall output reference voltage variation of $\pm 3.3\%$ overall corner cases. The total resistance of the circuit resistors is 581.25 KOhm which is lower than the total resistance which is used in [7, 8, 16] (1, 3.996 and 1.529 MΩ, respectively). In the case that the V-to-I converter was avoided and the topology in [3] (Figure 1) was used, the total resistance of the circuit resistors would have exceeded 1.75 MΩ for the same bias current of PMOS current sources, thus having the same current copy error. The latter implies that area reduction can be achieved by employing a V-to-I converter since only one large resistance is used instead of two for producing the CTAT-type current under the condition that the V–I converter consumes relatively small die area.

In the voltage reference circuits reported in the literature that were described above, several types of operational amplifiers have been used; however, to our best knowledge the use of rail-to-rail operational amplifiers have not been employed although advanced circuit techniques exist at low supply voltage [23–26]. In the proposed voltage reference circuit, a folded cascode operational amplifier with an NMOS input stage and a rail-to-rail output stage is employed (Figure 3) instead of a simple two-stage operational amplifier. The NMOS input stage allows for handling large input common mode voltages such as the emitter-base voltage (V_{EB}) of the substrate bipolar p-n-p devices while the rail-to-rail output stage makes efficient use of the supply voltage since it increases the output swing nearly up to the supply rail. As the PMOS current sources PM1, PM2, PM3 in Figure 2 are biased in the weak inversion region, their gate voltages have only few millivolts difference from the supply voltage. When the temperature is very low the voltage V_{EB} becomes very high thus the minimum supply voltage of the circuit increases. At the lowest supply voltage of 0.9 V both OA1 and OA2 should be able to drive the devices PM1, PM2, PM3 (Figure 2) even when temperature approaches -40°C. The rail-to-rail output stage of OA1 and OA2 satisfies the latter requirement under these conditions. This effect becomes harder to compensate at the ff (fast, fast) corner case where the bias current increases and the minimum supply voltage of the circuit reaches its maximum value. In this way, the circuit behavior is enhanced at low temperatures and proper operation is ensured with good stability at temperatures as low as -40°C when supply voltage is limited to 0.9 V.

The output stage is formed by the devices NM7-NM9 and PM5-PM8 and can be found in [24]. Class AB output stage topologies can also be found in [25, 26]. Using Class-AB Feedback Biasing (FBB), the push and pull currents are measured and compared with a reference bias current which is delivered by PM11. If the biasing is not correct in a class-AB relation ($I_{push} \cdot I_{push} = I_q$), then the output transistors receive a correction signal from a feedback signal provided by the drains of NM6a and NM6b. The measurements transistors (here: NM8 and PM7) are part of the so-called Minimum Current Selector Circuit which is formed by PM5-PM7, NM7 and NM8 [23]. The device PM4 is split into PM4a and PM4b. Similarly, PM6 is split into PM6a and PM6b. In this way,

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a folded mess is composed that represents the implementation of the floating voltage V_{AB} of the Class AB feedback control.

The operational amplifier gain should be high for better calibration. However, when the gain is set too high it may cause oscillations over process and supply voltage variations. This is possible due to the fact that the operational amplifiers OA1 and OA2 drive the large PMOS devices PM1, PM2 and PM3, PM4, respectively (Figure 2), thus they are loaded by very high capacitances in the range of 5 pF. For this reason the DC voltage gain of OA1 and OA2 was selected to be about 76 dB (at the typical corner case, 27°C, 1 V). Furthermore, in [13] a large external capacitor of 0.1 μF was necessary in order to eliminate the resulted oscillations for a DC voltage gain of 95 dB. The selected moderate voltage gain of 76 dB for our operational amplifier design ensures the stability of the total circuit without having to use a large miller capacitors or external components. Furthermore, operational amplifiers OA1, OA2 are biased with a PTAT current, which is provided by devices NM2 and NM3, respectively thus a relatively constant voltage gain is achieved over temperature variations. The folded cascode topology of the first stage of the operational amplifier enhances the PSRR of the proposed reference voltage generator. Although it is not shown in Figure 3, a power down circuit is included in the design of OA1, OA2 such that the total biasing current drops in the range of nA when it is shut down and the output of OA1, OA2 is set at V_{dd}. This implies that when the shut-down circuit of OA1 and OA2 is activated it forces the voltage reference circuit to shut down as well, due to the fact that the outputs of OA1, OA2, set at V_{dd}, are connected at the PMOS devices of the circuit. In addition, the use of the rail-to-rail output stage guarantees good linearity for the PTAT and CTAT generated currents over supply voltage variations.

For low supply voltage operation below 1 V, all PMOS devices of the circuit which play the role of current sources need to have very low effective voltage, $V_{\mathrm{ds,sat}}$, of about 80 mV to 100 mV. Thus, large device widths are employed. The bipolar devices B1, B2 must have large emitter areas for maintaining small emitter–collector voltages, V_{EC} such that more headroom is available. Moreover, in order to provide relatively high PSRR up to 50 KHz, a capacitor C is placed at the output of the reference voltage generator with a total capacitance of 6 pF.

The devices NM4, NM5 and PM7 form the voltage reference generator start-up circuit which can be found in [16]. At start-up, the current via B1, B2 may be equal to zero since there are two solutions for the conventional bandgap circuit core. In the case that the output voltage is reduced significantly due to the zero current flowing via B1, B2 the drain voltage of NM4 which is loaded by PM7 increases forcing NM5 to conduct high current, thus pulling down the gate voltage of PM1, PM2. Consequently, the current via B1, B2 increases and reaches the anticipated, non zero value. The devices NM4, NM5 and PM7 are designed with small dimensions so as not to conduct a large amount of current when the voltage reference generator works properly after start-up.

3. IMPLEMENTATION AND POST-LAYOUT SIMULATION RESULTS

The performance summary of the presented sub-1V supply voltage reference generator is given in Table I. In Figure 4, the reference voltage versus the supply voltage is depicted for different process corners at the temperature of 27°C. The proposed voltage reference generator supply voltage can vary from 0.9 to 1.5 V with a supply voltage sensitivity of 0.74% at the typical corner case and 27°C. The worst corner case supply voltage sensitivity is 1.12%.

In Figure 5, the reference voltage versus temperature is shown for different process corners cases at $V_{\mathrm{dd}} = 1$ V. The typical TC in the range between −40 and 125°C equals 23.66 ppm/°C. The performance deteriorates at sf (slow-fast) and fs (fast-slow) process corner cases. However, the total output voltage reference variation overall process corners and supply voltage variations in the wide temperature range of −36 and 125°C is limited to ±3.3%. The total power consumption equals 208 μW.

In Figure 6, the PSRR versus frequency is given for supply voltages of 0.9, 1 and 1.1 at 27°C. For these supply voltage levels, the PSRR at dc equals 32.53, 53.9 and 48.41 dB, respectively, at 27°C.

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Table I. BGR post-layout simulated performance summary.

Quantity	Post-layout simulated data
Process	TSMC Standard 90-nm CMOS
Devices	MOSFET 1 V, $V_{TN} = 0.25 - 0.35\,V$
Nominal supply voltage	1 V
Power dissipation	208 μW
V_{ref} at 27°C	510 mV
Temperature range over nine different cases for process and supply voltage (±10%) variations	−36 to 125°C
Temperature range for the typical corner case	−40 to 125°C
TC in the range between −40 and 125°C (typical)	23.66 ppm/°C
Absolute variation, $\Delta V_{ref}/V_{ref}$ (%), over nine different cases for process and supply voltage variations (±10%) between −36°C and 125°C	±3.3% @ $-36°C < T < 125°C$
Output reference voltage sensitivity for 0.9–1.5 V at 27°C (typical/worst)	0.74% / 1.12%
PSRR (dB) at 27°C	52.78
V_{ref}, integrated noise @ BW = 1 GHz at 27°C	257 μV
Stability $3\sigma_{TOTAL}/\bar{V}_{ref}$ (%) (−36, 27, 125°C), (0.9, 1, 1.1 V)	2.64
Effective area	232.30 μm × 211.84 μm or 0.0492 mm^2
Total area including dummy components and bondpads	284.68 μm × 233.15 μm or 0.066 mm^2

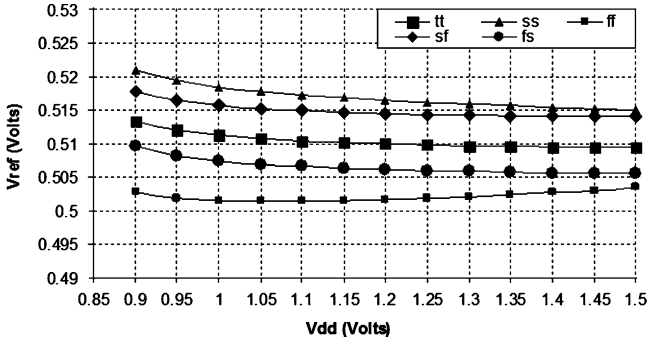

Figure 4. Reference voltage versus supply voltage for different process corners at 27°C.

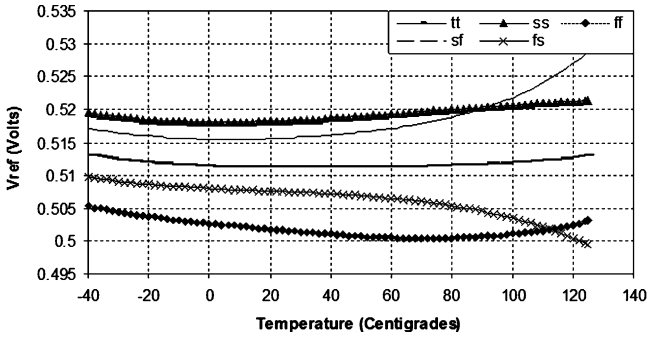

Figure 5. Reference voltage versus temperature for different process corners at $V_{dd} = 1V$.

In Figure 7, the operational amplifier open loop gain versus frequency is shown at the typical corner case at 27°C that is equal to 76.36 dB at dc. The open loop gain bandwidth product equals 2.7 MHz for a capacitive load of 10 pF. The post-layout performance summary of the operational amplifier is summarized in Table II. It exhibits an offset voltage of 635 μV, an RMS noise voltage of 106 μV for an integration bandwidth of 1 GHz.

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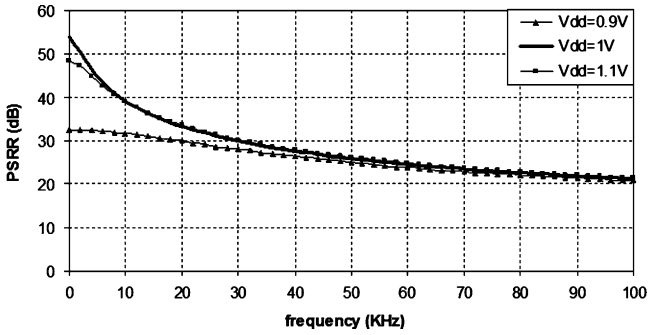

Figure 6. Power Supply Rejection Ratio versus frequency for supply voltages of 0.9, 1 and 1.1 V at 27°C.

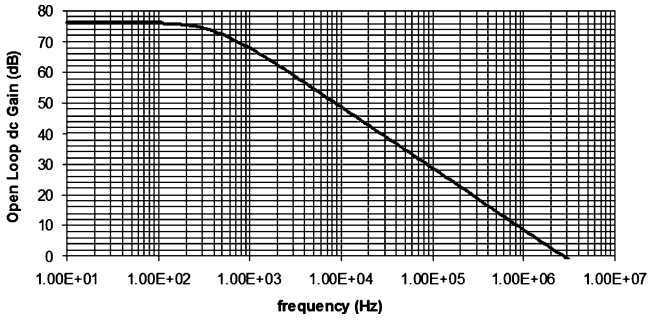

Figure 7. Operational amplifier open loop gain versus frequency.

Table II. Operational amplifier post-layout simulated performance summary.

Quantity	Post-layout simulated data
Process	TSMC Standard 90-nm CMOS
Nominal supply voltage	1 V
Total current	87 μA
Open loop DC gain	76.36 dB
Open loop GBP	2.7 MHz at C_{load} of 10 pF
Offset voltage	635 μV
Phase margin	92°
RMS V_{noise}, integration BW=1 GHz	106 μV

Monte Carlo simulations have been performed for three different conditions of temperature (−36, 27 and 125°C) and for three different conditions of supply voltage (0.9, 1, 1.1 V) for the calculation of the total 3σ and the mean value of V_{ref} of the proposed sub-1V supply voltage reference generator. As a result, there are nine matrix simulation conditions. Each Monte Carlo simulation has been performed for 50 samples. The mean value, the standard deviation of the resulted samples ($3 \times 3 \times 50$) of V_{ref} and the percentage frequency of appearance of each sample in 16 different intervals (2 mV each) from 498 to 530 mV are given in Figure 8. The total 3σ deviation of V_{ref} equals 13.5 mV and the average value equals 512.4 mV. Therefore, the resulted stability, $3\sigma/V_{ref}$, of the proposed sub-1V supply voltage reference generator equals to 2.64%. In Figure 9, the layout view of the proposed sub-1V supply CMOS voltage reference generator is presented. It consumes an effective layout area of 0.0492 mm^2 (232.30 μm × 211.84 μm).

A performance comparison is summarized in Table III between the post-simulation results of the proposed circuit and the measured or post-layout simulation results ([6, 8–10, 17]) of other voltage references reported in the literature. The presented sub-1V supply CMOS voltage

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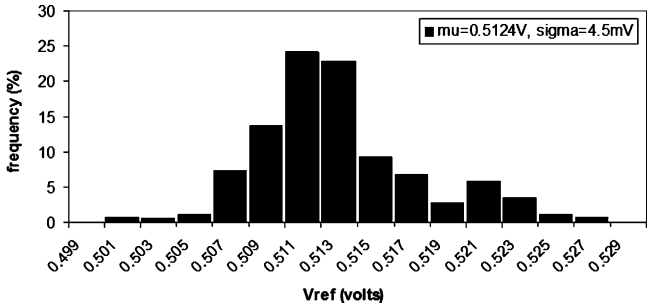

Figure 8. Distribution of V_{ref} based on Monte Carlo simulation results of the proposed sub-1V supply voltage reference generator. Three different simulation conditions of temperature (−36, 27 and 125°C) and three different simulation conditions of supply voltage (0.9, 1, 1.1V) are taken into account.

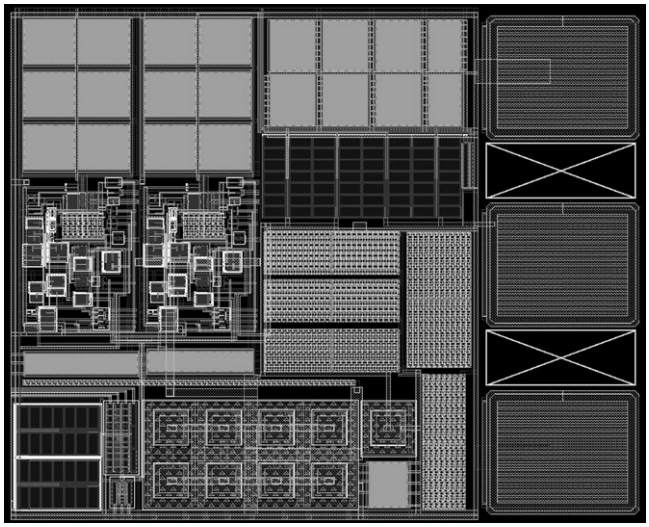

Figure 9. Proposed sub-1V supply CMOS voltage reference generator layout view.

reference generator operates in the widest temperature range of −40 to 125°C achieving a TC of 23.66 ppm/°C. The same wide temperature range is achieved by the proposed bandgap circuit presented in [12] with a smaller TC, yet it operates at a higher nominal supply voltage of 3 V and it consumes higher area. Furthermore, as it can be seen in Table III, the sub-1V bandgap references reported in [20, 21] achieve better overall performance in the temperature range of −40 to 125°C at the expense of higher die area. The absolute total reference voltage variation over process corners in [9] equals to ±8.5%, whereas the circuit presented in this paper exhibits a total absolute variation of ±3.3% in a much wider temperature range. Although our design solution draws current that is among the highest ones reported due to the presence of two operational amplifiers, it occupies low area and it is capable of low voltage operation between 0.9 and 1.1 V. Therefore, in the proposed design approach, power consumption is traded for low layout area. In Table III, $V_{dd,min}$ is defined as the minimum supply voltage where the circuit can be stable, yet the reported performance is not measured at this low supply voltage but at V_{dd} instead. It should be noted that the power consumption of 208 μW is not an obstacle for several sub-1V applications such as PLL, DLL for DDR2–DDR3 PHYs and SERDES systems since it remains negligible when compared with other sub-blocks of these systems such as the VCO and the prescaler. On the contrary, the low total absolute variation of the reference voltage in the wide temperature range between −40 and 125°C for a 10% variation of the 1 V nominal supply voltage and the low layout area was the prime design goal for the proposed sub-1V supply voltage reference generator. The total 3σ deviation

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Table III. Performance comparison of bandgap references around 1V.

Reference	Technology	$V_{dd,min}$ (V)	V_{dd} (V)	T_C (ppm/°C)	ΔT (°C)	I_{dd} (μA)	DC PSRR (dB)	LNR (%)	$3\sigma/\bar{V}_{ref}$ (%)	Area (mm^2)
[3]	0.4-μm CMOS	0.84	2.2–4	N/A	27–125	2.2	N/A	N/A	2.9	0.1
[5]	0.8-μm BiCMOS	>0.95	1	N/A	0–80	92	N/A	0.014	N/A	0.3*
[6]	0.18-μm CMOS	—	1–2.4	18.5	−45 to 90	0.83	N/A	1	N/A	0.008
[7]	1.2-μm CMOS	—	1.2	119	−25 to 125	3.6	>40	N/A	3.65	0.23
[8]	90 nm CMOS	1	1.05–1.35	N/A	−20 to 90	1.3	N/A	N/A	N/A	N/A
[9]	0.18-μm CMOS	—	1–2.2	6.6	−10 to 70	160	N/A	0.16	N/A	N/A
[10]	0.13-μm CMOS	—	0.5	2.2	−40 to 100	0.08	14	N/A	N/A	0.00025
[11]	0.35-μm CMOS	—	3–3.3	10	−20 to 100	230	N/A	N/A	N/A	0.0204
[12]	0.5-μm CMOS	0.95	3.3	17	−40 to 125	10	N/A	N/A	N/A	0.109
[13]	0.5-μm CMOS	—	4.5–5	32	−10 to 80	204	N/A	1	N/A	0.0936
[16]	0.35-μm CMOS	0.9	1–1.6	N/A	−20 to 50	4.3	>40	N/A	4	0.13
[17]	0.18-μm CMOS	—	1.2–1.4	20	0–100	5	>50	N/A	N/A	0.033
[18]	0.35-μm CMOS	0.85	0.9–1.5	N/A	0–140	10	N/A	N/A	N/A	N/A
[19]	0.18-μm CMOS	—	1.35–1.5	N/A	0–80	146	47	N/A	N/A	0.057
[20]	0.5-μm BiCMOS	0.85	0.85–5.5	11[¶]	−40 to 125	21	110	N/A	0.56[†]	0.4*
[21]	0.5-μm BiCMOS	0.85	1–5	11[¶]	−40 to 125	20	N/A	0.0048[§]	0.56[‡]	0.4*
This work	90-nm CMOS	<0.9	0.9–1.5	23.66	−40 to 125	208	52.78	0.74	2.64	0.066*

$V_{dd,min}$ is defined as the minimum supply voltage where the circuit can be stable. The reported performance is not measured at this low supply voltage. References [6, 8–10, 17] report post-layout simulations results.
*Including pads.
[†]Converted from $V_{ref} \pm 3 \cdot \sigma = 190.9\,mV \pm 1.083\,mV$ to $3 \cdot / V_{ref} \cdot 100 = 0.56\%$.
[‡]Converted from $V_{ref} \pm \sigma = 190.9\,mV \pm 0.361\,mV$ to $3 \cdot / V_{ref} \cdot 100 = 0.56\%$.
[§]Converted from 48uV/V to 0.0048%.
[¶]Measured at a supply voltage of 1V for 32 test samples.

equals 13.5 mV. The PSRR performance is higher than the PSRR reported in [7, 10, 16, 17, 19] and lower than the PSRR reported in [20, 21].

4. CONCLUSION

A sub-1V supply voltage reference generator was presented that has been designed and implemented in TSMC 90-nm digital CMOS process. It consists of a conventional bandgap core, where a PTAT current flows and a voltage to current converter that transforms the CTAT emitter-base voltage of the core bipolar device into a current with negative TC. The two currents with opposite temperature dependency are added producing a constant, temperature independent current which in turn is linearly transformed to a reference voltage via a resistor. The circuit includes two operational

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amplifiers with a rail-to-rail output stage for enabling stable and robust operation overall process and supply voltage variations especially at very low temperatures and low supply voltage. The proposed circuit exhibits a total variation of the output reference voltage equal to ±3.3% overall process and supply voltage (±10%) variations in the wide temperature range between −36 and 125°C and a total 3σ standard deviation of 13.5 mV for an average output reference voltage of 512 mV ($3\sigma/\bar{V}_{\text{ref}}$ of 2.65%). In addition, a PSRR of 52.78 dB and a TC of 23.66 ppm/°C in the range between −40 and 125°C at the typical corner case of 1 V were achieved. Effort was made in order to achieve as small as possible the die area by limiting the number and the value of the resistors of the circuit without sacrificing performance. The employment of the V-to-I converter for the CTAT-type current production enables the use of only two large resistors with a total resistance on the order of half MΩ. As a result, area reduction can be accomplished by employing a V-to-I converter since only one large resistor is used instead of two for providing the CTAT current, under the condition that the V–I converter consumes relatively small die area. The proposed circuit can be used in applications where sub-1V supply voltage is necessary (e.g. PLL, DLL for DDR2–DDR3 and SERDES PHYs, etc.).

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