

Design and implementation of a DCS 1800 receiver

FOTIS PLESSAS, PASCHALIS SIMITSAKIS,
GRIGORIOS KALIVAS

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This paper presents the design and implementation of a radio receiver front-end using discrete components, commercial ICs and incorporating a custom designed image rejection (IR) mixer. The design and implementation of the IR network is very critical, demanding and requires accurate matching of the quadrature branches. The measured results demonstrate that it is practically feasible to implement such a subsystem with realistic specifications that can satisfy the demands for the radio front-end of a DCS 1800 receiver.

Key words: DCS receiver, image rejection mixer, polyphase filter, I/Q demodulator

1. INTRODUCTION

The design and development of receivers for a range of wireless standards such as GSM, Bluetooth, DECT, IEEE802.11 etc. has attracted much attention during recent years. This comes from increasing demands in developing products for cellular, mobile, personal and wireless LAN applications.

Most of the work focuses on the design and development of the complete receiver in the form of an integrated circuit [1], [2], [3], [4].

The objective of this paper is to design and develop a DCS 1800 receiver using discrete components and commercial ICs. This implementation approach serves two purposes: a) to provide flexibility for fine-tuning of sensitive subsystems in the front-end chain and b) to demonstrate that a complete radio front-end satisfying the standard's specifications can be implemented using discrete components and ICs. In addition, this provides a fast and inexpensive way to build and test prototypes for future integration.

As mentioned above, the critical issue of matching the in-phase and quadrature components of the image rejection mixer must be handled carefully, as it can be easily shown [5], [6] that mismatches of passive (resistors, capacitors) or active components (mixers) can result in substantial reduction of the image rejection capability of the receiver.

The authors are with the Department of Electrical and Computer Engineering, University of Patras, Rion 26500, Greece. e-mail: plessas@ee.upatras.gr
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In section 2 we present the system electronic specifications as derived from the ETSI standard requirements. Section 3 gives the overall receiver system design/planning and presents the chosen architecture along with the major constituting components. Section 4 outlines the implementation of the subsystems and the overall receiver, while section 5 gives measurement results. Finally, some conclusions are outlined in the concluding section 6.

2. SYSTEM SPECIFICATIONS

The ETSI standard committee has specified the use of 900 MHz GSM band and the 1800 MHz DCS band for voice and data services [7]. DCS 1800 has evolved from the GSM standard. The main differences are transmitting power levels and operating frequency band. In both cases the GMSK modulation is adopted. DCS 1800 has 374 frequency channels (transmitting at 1710-1785 MHz, receiving at 1805-1880 MHz), the channel spacing is 200 KHz and the gross bit rate is 270.833 Kb/s.

ETSI has also specified receiver characteristics associated with blocking interference and intermodulation distortion issues [7]. At the same time it provides specifications regarding the transmitter/receiver performance in terms of sensitivity and reference interference levels.

Table I illustrates the most important requirements affecting the system design and implementation.

Table I - Receiver Characteristics for DCS 1800

Max Input	-23 dBm (for 0.1% BER in static channel)
Reference sensitivity	-102 dBm (8% BER in TU50 channel)
Co-channel interference	-9 dB with respect to wanted signal at -82 dBm (8% BER in TU50 channel)
Adjacent channel interference	9 dB with respect to wanted signal at -82 dBm (8% BER in TU50 channel)
Alternate channel interference	41 dB with respect to wanted signal at -82 dBm (8% BER in TU50 channel)

BER requirements impose a 10^{-3} error rate in static conditions. When the propagation channel is characterized by dispersion, a 2% BER is allowed in traffic channels for speech (TCH). A GMSK modem with coherent demodulation achieves this BER at $SNR = 10$ dB (including implementation losses). Consequently, the required noise figure of the implemented system is:

$$NF = P_s - SNR_r - 10 \log(BW) + 173.83 = 8.8 \text{ dB} \quad (1)$$

where, P_s is the equivalent receiver noise power, SNR_r represents the required signal-to-noise ratio, -173.83 dBm is the thermal noise level at 25°C at 1 Hz bandwidth and BW is the system bandwidth in Hz.

Depending on the value of the IF frequency, the required image rejection can vary from 35 dB (for low IF architecture) to almost 60 dB for a typical IF in the range of 5-80 MHz. In both cases the needed amount of image rejection stems from the requirements for blocking characteristics for in-band or out-of-band blockers [ETSI TS-100-910].

Taking into account the required sensitivity (-102 dBm) and the maximum permitted signal level

(-23 dBm), the dynamic range of the receiver should be 79 dB. To implement such a value an AGC is necessary.

To obtain the overall IIP3 specification the intermodulation characteristics have to be taken into account. For this issue ETSI specifies that a useful signal with power of -99 dBm should be demodulated correctly in the presence of 2 interferers, 800 KHz and 1600 KHz away, with a power of -45 dBm. Taking these into account the IIP3 is calculated to be equal to [5]:

$$IIP_3 = P_{in} + (P_{in} - P_m + SNR)/2 \quad (2)$$

where P_{in} is the power of the interferer, P_m is the useful signal power and SNR is the required signal to noise ratio for acceptable performance. Taking into account that the required SNR is approximately 10 dB, it turns out that the overall IIP3 is -8.5 dBm.

Finally, in-band blocking is used to estimate the 1-dB compression point CP(1dB). In the case of DCS 1800 the in-band blocking at 3 MHz offset is equal to -23 dBm. Taking another 3 dB losses immediately after the antenna, the overall CP(1dB) is -26 dBm.

3. SYSTEM PLANNING

The receiver topology is shown in Fig.1. A superheterodyne architecture is chosen with a 1st IF frequency of 82.8 MHz. This allows the use of off-the-self components while at the same time it distributes the high overall image rejection in both the front-end filter and the image rejection mixer. A 2nd IF frequency of 400 KHz is chosen which permits direct digital processing at the In-phase (I) and Quadrature (Q) outputs of this stage.

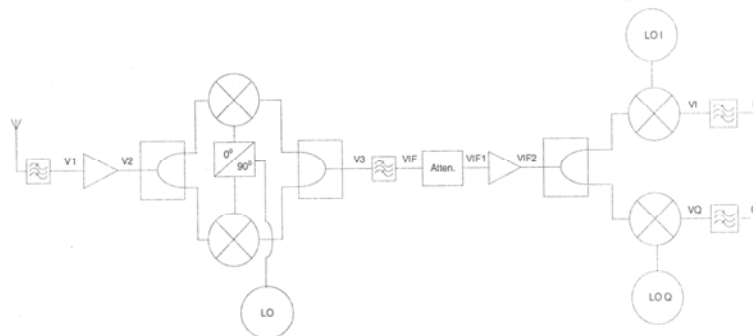
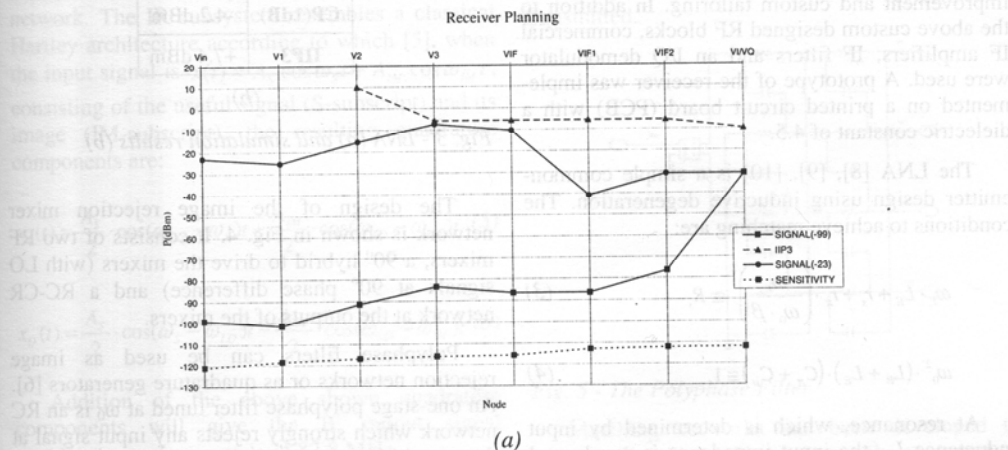


Fig. 1 - Receiver Block Diagram

Following the antenna there is a band selection filter to reject out-of-band interference signals. This filter is usually equivalent to a 2nd order Butterworth filter and its maximum insertion loss should not exceed 2.5 dB. Following the filter there is an LNA, which gives a gain and NF of 10.7 dB and 1.5 dB respectively. The output of the LNA is down-converted using an RF image rejection (IR) mixer which is one of the most critical components of the overall radio receiver. More specifically, it needs to amplify the signal by 8 dB while maintaining a NF less than 10 dB (since the overall NF should be lower than 8.8 dB). It also should exhibit a reasonably good linearity as the mixer is the point in the receiver chain where most of the non-linearities are produced. So, a CP(1dB) of -5 dBm and an IIP3 of 5 dBm are specified for the IR mixer. The last but very important issue is the image rejection capability of

the mixer. According to the application characteristics resulting from the DCS 1800 specifications the image rejection should be higher than 50 dB. The band selection filter after the antenna provides an image rejection in the order of 25 dB. This leaves a figure of 25 dB image rejection to be met by the IR mixer. As shown in detail in the following section, the IR mixer consists of two RF mixers, a polyphase filter (to create the 90° phase difference between the two LO paths), an RC-CR network and a power combiner.

In this work we have given much attention in implementing an IR mixer using modern polyphase filter design techniques. This will demonstrate the effectiveness of designing with discrete components such sensitive subsystems of the radio receiver.



	Overall	V1	V2	V3	VIF	VIF1	VIF2	V1/VQ
NF (dB)	8.8	2.5	1.5	9	3	4	3.3	8
Gain (dB)	-6.8 to 68.2	-2.5	10.7	8	-3	-30 to 0	10	0 to 45

(b) Fig. 2 - Receiver Planning

The IR mixer is followed by an IF filter performing the system filtering. It is tuned at 82.8 MHz with properties similar to those of a 2nd order Butterworth filter and a typical loss of 3 dB.

A gain control system follows the SAW filter and is realized using a voltage-controlled attenuator and an IF amplifier. The whole system should be able to achieve a -30 to 10 dB of controllable gain. The amplifier has a gain of 10 dB, a NF of 3.3 dB, an output CP(1dB) of +12 dBm, an OIP3 of +23 dBm.

In the final stage an I/Q demodulator should be used to down-convert at the second IF of 400 KHz and provide the I and Q channels. This subsystem should provide a gain of 0 to 45 dB with a NF of 8 dB. In addition, the CP(1dB) is -10 dBm while the IIP3 is +2.2 dBm. Low pass filters are used at the output to further reduce the system noise and eliminate the upper sideband.

Figure 2a gives the overall receiver planning in terms of signal level (min and max), sensitivity and IIP3. Points marked as V1, V2, V3, VIF etc.

correspond to input (or output) stages in the receiver block diagram (Fig. 1). Figure 2b shows the NF and gain values for each component in the receiver chain.

Summing up the important design features of the radio receiver we have an overall NF of 8.8 dB, a total IIP3 of -9.9 dBm and a total conversion gain of -6.8 dB (for the highest power input) to 68.2 dB (for the lowest input).

4. SYSTEM IMPLEMENTATION

To match the specifications and implementation approach presented in the previous section, special attention should be paid to the development of the high frequency subsystems. Discrete components are used for implementing most of the subsystems such as the LNA, the image rejection mixer and the polyphase filter. This provides a lot of flexibility in the design and allows for further improvement and custom tailoring. In addition to the above custom designed RF blocks, commercial IF amplifiers, IF filters and an I/Q demodulator were used. A prototype of the receiver was implemented on a printed circuit board (PCB) with a dielectric constant of 4.5.

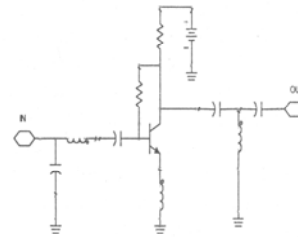
The LNA [8], [9], [10] is a simple common-emitter design using inductive degeneration. The conditions to achieve matching are:

$$\omega_r \cdot L_E + r_x + r_\pi \cdot \left(\frac{\omega_r}{\omega_0 \cdot \beta} \right)^2 \cong R_s \tag{3}$$

$$\omega_0^2 \cdot (L_B + L_E) \cdot (C_\pi + C_\mu) \cong 1 \tag{4}$$

At resonance, which is determined by input inductance L_B , the input impedance is purely real and equal to $\omega_r L_E$. This simple structure offers low noise and moderate gain. We used a commercial bipolar transistor, which offers very good per-

formance concerning noise and linearity. The LNA and the simulation results are presented in Fig. 3. Feedback and collector resistors are connected for biasing purposes.



(a)

Gain	10.7 dB
NF	1.5 dB
VSWR	1.5
CP(1dB)	-4.2 dBm
IIP3	+7.4 dBm

(b)

Fig. 3 - LNA (a) and simulation results (b)

The design of the image rejection mixer network is shown in Fig. 4. It consists of two RF mixers, a 90° hybrid to drive the mixers (with LO signals at 90° phase difference) and a RC-CR network at the outputs of the mixers.

Polyphase filters can be used as image rejection networks or as quadrature generators [6]. An one-stage polyphase filter tuned at ω_0 is an RC network which strongly rejects any input signal at the ω_0 within a small bandwidth. To increase the bandwidth an m-stage network must be employed. The rejection is now improved and the bandwidth of operation wider.

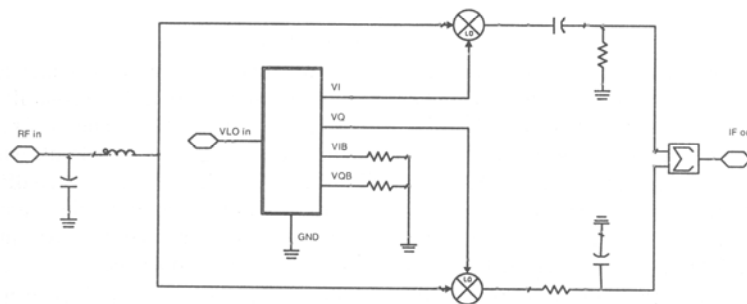


Fig. 4 - The image rejection mixer network

In our application a polyphase filter is used as a quadrature generator for the LO signal. Two stages are required for broad-band quadrature, wide-band gain matching and reduced sensitivity to components mismatch. A two-stage passive polyphase filter [3], [6] as shown in Fig. 5 was designed and implemented. It is driven by a differential signal (1887.8 to 1962.8 MHz) through a balanced-to-unbalanced (balun) transformer at the input and generates the quadrature outputs.

The RF signal is splitted into two equal signals which are multiplied at the RF mixers by the quadrature LO outputs of the polyphase filter (Fig. 4), producing two IF signals at 82.8 MHz. These signals suffer a $\pm 45^\circ$ shift by the RC-CR network tuned at ω_{IF} and are added. The unwanted image frequency signal (1970.6 to 2045.6 MHz) is eliminated while the useful signal (1805 to 1880 MHz) is not affected by the image rejection mixer network. The IR subsystem resembles a classical Hartley architecture according to which [5], when the input signal is $x(t) = A_s \cos \omega_s t + A_{IM} \cos \omega_{IM} t$, consisting of the useful signal (S-subscript) and its image (IM-subscript), the resulting quadrature components are:

$$x_I(t) = \frac{A_s}{2} \cdot \cos(\omega_{LO} - \omega_s)t + \frac{A_{IM}}{2} \cdot \cos(\omega_{LO} - \omega_{IM})t \quad (5)$$

$$x_Q(t) = \frac{A_s}{2} \cdot \cos(\omega_s - \omega_{LO})t - \frac{A_{IM}}{2} \cdot \cos(\omega_{LO} - \omega_{IM})t \quad (6)$$

Addition of the above shown quadrature components will give the IF output signal $x_{IF}(t) = A_s \cdot \cos(\omega_{LO} - \omega_s)t$ at 82.8 MHz.

Simulation results showed an image rejection exceeding 60 dB, a conversion loss of 10 dB, a CP(1dB) of 12 dBm and an IIP3 of 22 dBm in the ideal case. Mismatches produced during the implementation and the inaccurately modeled voltage adder, which has infinite input impedance and zero output impedance, will degrade the overall performance of the IR network.

The primary objective of the implementation was to demonstrate sensitivity, linearity and image rejection features of the receiver. For this reason and in order to keep the physical realization as simple as possible only the IF amplifier was inserted in the IF chain. The IF amplifier has a gain

of 10 dB, an output CP(1dB) of 12.5 dBm, an OIP3 of 27 dBm and a NF of 3.3 dB.

The I/Q demodulator is a commercial component which combines the functionality of an I/Q modulator, an I/Q demodulator, a PLL and a variable gain (-17 to 61 dB) amplifier. The NF is 8 dB with an output CP(1dB) of -14.1 dBm and an OIP3 of 2.2 dBm. A lowpass filter with a cutoff frequency of 7.7 MHz is also included.

At the front end, a bandpass filter was used, equivalent to a 2nd order Butterworth filter with a resonant frequency of 1842.5 MHz, a bandwidth of 75 MHz and a loss of 2.5 dB. The IF filter also exhibits similar performance to a 2nd order Butterworth, with a resonant frequency of 82.8 MHz, a bandwidth of 24 kHz and a loss of 4 dB. Although the system bandwidth is 200 KHz, the chosen bandwidth does not affect much on the rest of the system when voice information is being transmitted.

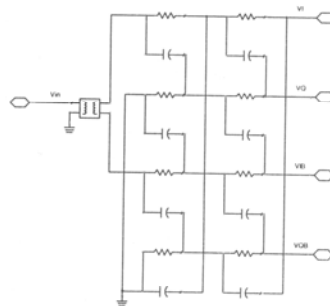


Fig. 5 - The Polyphase Filter

Matching networks has been developed to improve the mismatching between the components. Under these conditions the maximum controllable voltage gain is 65 dB and the NF is 8.8 dB. The CP(1dB) is -21 dBm, the IIP3 is -10 dBm and the image rejection is 60 dB. These results were quite satisfactory and thus the receiver has been implemented.

5. TESTING AND MEASUREMENT

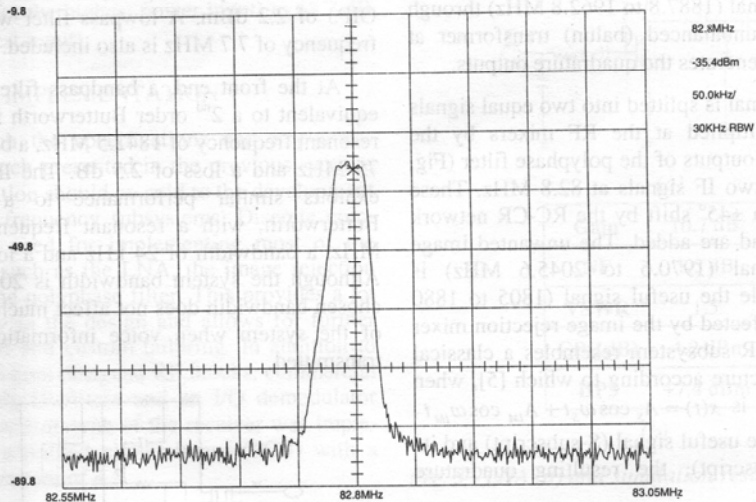
In this section we present briefly the testing apparatus and give measurement results.

One signal generator is used to feed the system with an RF input signal (HP8620C) and two others are used as local oscillators at the IR mixer (HP8648C) and the IF mixer (HP8620A). The

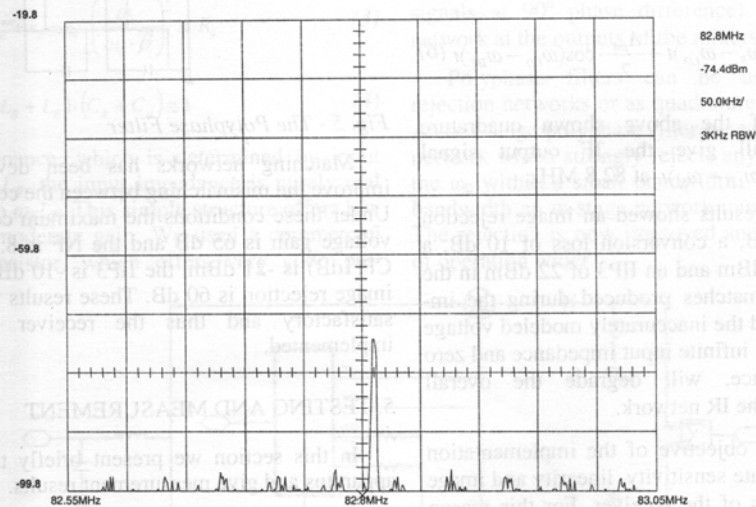
measurements have been performed using a TEK 2712 spectrum analyzer and a TDS 520 digital oscilloscope from Tektronix.

Figure 6 demonstrates measurement results at the IF. A -37 dBm RF input signal at 1846 MHz

produced -29 dBm at the input of image rejection network. At the output of the image rejection network the signal was -41 dBm at 82.8 MHz. This power is lower than the expected because of the insufficient driving power of the RF mixers.



(a)



(b)

Fig. 6 - IF amplifier's output (a) and IF amplifier's output for image input (b)

The measured power at the output of the IF amplifier was -35.4 dBm and the signal spectrum is as shown in Fig. 6(a). There is a slight difference between the simulated and measured results because of the inaccurate modeling of the power combiner at the output of the IR network and the implementation losses.

Figure 6(b) shows the output of the IF amplifier when an unwanted image frequency is detected at the input of the receiver. The power of the image signal is -74.4 dBm, resulting in an image rejection of 39 dB. The rejection is 10 dB lower than the minimum specification value but still satisfactory.

Potential implementation losses in preceding stages accumulated to this power penalty. This is also due to the insufficient models for passive and active components.

Measurement of the quadrature signals at the output of the receiver gave -31.2 dBm at 400 kHz as shown in Fig. 7. The components at the right of the useful signal are the spurious generated by the receiver while the ones located at the left are related to the measuring instrument (DC and instrument-related image). The unwanted signals are more than 40 dB below the useful tone.

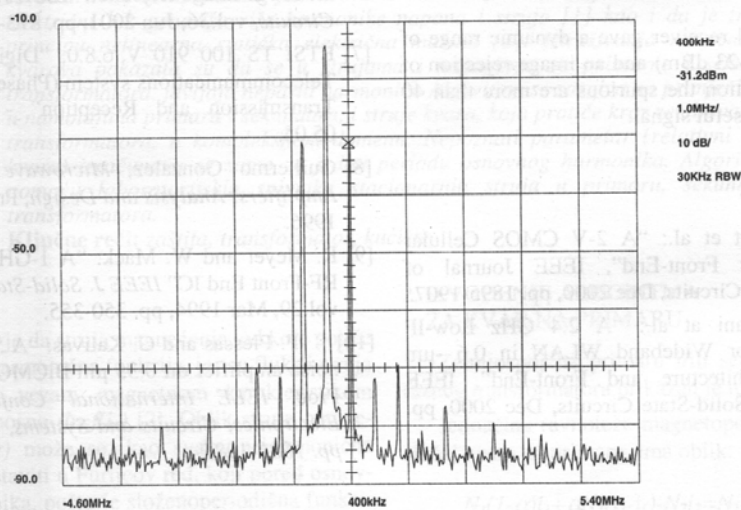


Fig. 7 - The output of the receiver

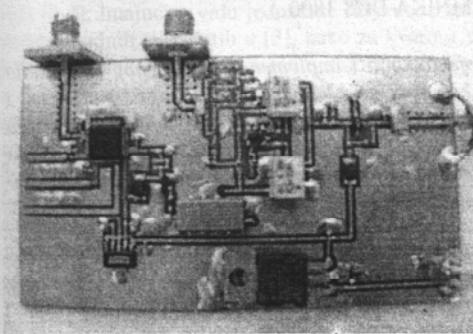


Fig. 8 - Photograph of the implemented prototype

Figure 8 illustrates the implemented prototype. The two LO signals are fed at the top of the picture through SMA connectors. The RF input (antenna) is located at the upper right hand side, whereas the three lines at the left represent the quadrature outputs and the receive AGC amplifier DC gain control input.

CONCLUSIONS

In this work, a DCS 1800 radio receiver was designed and implemented. A custom design was used for the high-frequency subsystem. This provided flexibility for fine-tuning and fast prototype implementation.

The receiver comprises of a low noise amplifier, an image rejection mixer network, a polyphase filter driven from the LO and IF off-the-self components (SAW filter, amplifier, I/Q demodulator). The measured results give a satisfactory performance and therefore the topology is very suitable for integration in an advanced SiGe or CMOS process.

The image rejection mixer network comprises the most critical subsystem because it must satisfy stringent demands for image rejection while maintaining good linearity and low noise figure. Simulation and subsequent implementation showed a very good performance in terms of image rejection making it suitable for on-chip implementation.

The overall receiver gave a dynamic range of 76 dB (-99 to -23 dBm) and an image rejection of 39 dB. In addition the spurious are more than 40 dB below the useful signal.

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