Microelectronics Journal 75 (2018) 61–67

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A high accuracy voltage reference generator

George Souliotis [a,*], Fotis Plessas [b], Spyridon Vlassis [c]

[a] Department of Electrical Engineering, Technological Educational Institute of Western Greece, Patras, Greece
[b] Department of Electrical and Computer Engineering, University of Thessaly, Volos, Greece
[c] Electronics Laboratory, Department of Physics, University of Patras, Patras, Greece

ARTICLE INFO

Keywords:
Voltage reference generators
Bandgap Voltage Reference
Constant current reference

ABSTRACT

A high-accuracy voltage reference generator is proposed in this paper. It has been designed in a CMOS 65 nm technology node, operating with a typical supply voltage of 1.2 V, which provides a reference voltage equal to 0.5 V. Measurement results of the fabricated chip show a reference voltage variation less than 0.04% over temperature range from −40 to 125 °C and less than 0.9% over temperature and supply voltage corners. The proposed design demonstrates a low noise output and good performance under mismatch. A current reference generator has been included in the design to provide a constant reference current. The measured variation of the reference current is about 1%.

1. Introduction

Analogue circuits are used in many electronic devices for several applications, such as communications, biomedical electronics, portable devices, computer systems and others. Analogue circuits however, are sensitive in variations of the supply voltage, the bias current, the temperature and the fabrication process. To reduce their sensitivity, a constant voltage reference or a constant current reference is required to bias the analogue circuits. A voltage reference generator produces a constant voltage independent of the temperature and supply voltage [1]. Implementations of voltage reference generators, known as Bandgap Voltage Reference (BGR) Generators, usually, were designed to generate a constant voltage around 1.26 V at 27 °C (300 K). This value is compatible with the silicon bandgap value [2,3] and it is suitable for BJT based circuits. Also, the reference voltage of 1.27 V was used in the first generation of MOS based circuits operating with higher threshold and supply voltage comparing with the modern circuits. As the constant reference voltage was 1.26 V the required supply voltage was greater than 1.4 V in order to achieve reasonable power supply rejection ratio (PSRR). However nowadays, these values of the supply and the reference voltages are too high for the recent circuits designed for portable devices, which must operate with much lower supply voltage. Therefore, the most recent voltage reference generators, not only operate under lower supply voltage but also, they generate lower reference voltage, as well. A typical value for the reference voltage is around 0.5 V, close to the threshold voltage of an NMOS transistor.

Several topologies have been proposed for voltage reference generators. BiCMOS topologies were introduced in Refs. [4–6], however they are rarely used in modern systems due to the high power consumption. Other CMOS based voltage generators -adopt special design techniques, such as the dynamic threshold MOS transistors (DTMOST) used in Ref. [7]. In this, the transistors must be designed with separated wells making the layout design large, prone to mismatches and requiring triple well CMOS technology nodes. In Ref. [8], the proposed sub-1V voltage reference generator uses native transistors, which require an extra mask and therefore the fabrication process is more expensive. In addition, the employment of native transistors may limit the porting ability to other technology nodes. Furthermore, in Ref. [8], the required operational amplifiers (OAs) operate with 2.1 V and thus, the advantage of the sub-1V operation is totally vanished. The circuit reports operation from 0 to 125 °C.

Some 1 V topologies are designed based on transistors operating in weak inversion region to reduce power consumption and to avoid the employment of bipolar PNP devices [9–20]. These topologies, although dissipate low power however, they offer operation in a relatively small temperature range, in some cases up to only 80 °C. In Refs. [21] and [22], low voltage, low power, topologies based on weak inversion operation are reported. An internal, VDD charge-pump doubler and a clocked switched-capacitor V_{BE} divider are used. Thus, a buffer is needed to drive high load currents, increasing the total power consumption. Reference voltage generators based on weak-inversion transistor are more sensitive in voltage variations or they are prone to instability requiring large

* Corresponding author.
E-mail addresses: gsoul@teiwest.gr (G. Souliotis), fplessas@e-ce.uth.gr (F. Plessas), svlassis@physics.upatras.gr (S. Vlassis).

https://doi.org/10.1016/j.mejo.2018.02.006
Received 16 December 2017; Received in revised form 6 February 2018; Accepted 26 February 2018

capacitors for compensation [23,24]. They may be suitable for extremely low power consumption systems, but they may not be suitable when the generated reference voltage drives a large load. Furthermore, most of them operate in relatively low temperature range. Topologies based on CMOS only transistors, with extended temperature range compared to others, are presented in Refs. [25,26]. Circuits based on more conventional topologies are proposed in Refs. [27–29]. Some of the topologies require high gain [24] or rail-to-rail operational amplifiers [28], which makes the design more complicated. A review for voltage reference generators takes place in Ref. [30] and start up considerations are studied in Ref. [31]. A study of the effect on the circuit operation under temperature variations is given in Ref. [32]. The most important property of the voltage references generators is the low dependency of the reference voltage under process, voltage and temperature (PVT) variations. Two other important properties are the stability and the driving capability.

A voltage reference generator is proposed in this paper, based on the two operational amplifiers topology presented in Ref. [28]. The architecture has been optimized through a detailed theoretical analysis in terms of performance, silicon area, and power consumption. Compared with [28], the proposed circuit does not employ rail-to-rail operational amplifiers, and thus, it is simpler in design and more compact in layout. The bias current of the operational amplifiers is properly selected to reduce the final output voltage variations. The proposed design does not require any external large capacitor for filtering or stability and this is an important improvement. During the theoretical analysis, small resistors have been chosen, making the layout significantly smaller compared with [28]. A current reference generator has been employed together with the voltage reference generator whereas the noise performance is also examined. Finally, the work from Ref. [28] reports only simulation results while we demonstrate the efficiency of the optimized architecture by implementing and validating it. Measurement results show very good agreement with simulation results, significant improvement in the performance compared to [28], and the effectiveness and robustness compared to other recent designs. In Sections 2 and 3 the proposed topology is studied and in Section 4, measurement and simulation results of the fabricated chip are provided. The conclusions are given in Section 5.

2. Circuit analysis of the proposed BGR

The electrical behavior of the semiconductor elements is significantly affected by the wide temperature variation. When a constant voltage is required, it can be generated by combing an electrical quantity with positive temperature coefficient (TC) with an electrical quantity with negative TC, as shown in Fig. 1. The first gives a Proportional-To-Absolute-Temperature (PTAT) quantity and the second a Complementary-To-Absolute-Temperature (CTAT) quantity.

The base-emitter voltage V_{BE} of a bipolar transistor has a negative TC about -2 mV/°C and the thermal voltage V_T has a positive TC of 0.085 mV/°C. Assuming that $V_{BE} \gg V_T$, the operation of the transistor is given by the known approximate equation,

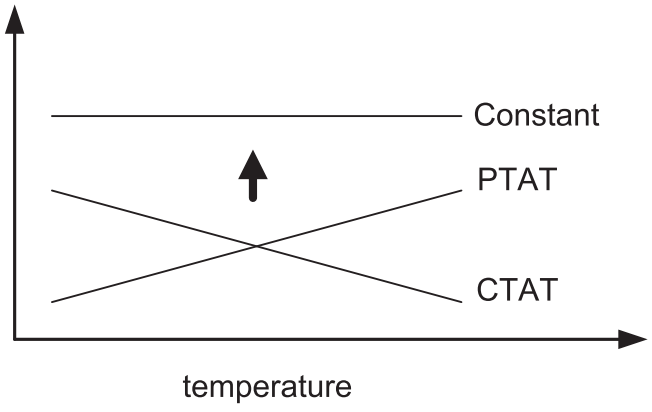

Fig. 1. Constant voltage generation by a PTAT and a CTAT voltage.

$$I_C = I_S \cdot e^{\frac{V_{BE}}{V_T}} \tag{1}$$

where, I_S is the reverse saturation current, $V_T = kT/q$, k is the Boltzmann constant, T is the absolute temperature and q is the electrical charge of an electron.

The topology of the BGR is shown in Fig. 2. The Operational Amplifier (opamp) OA1 biases properly the PMOS transistors M_1 and M_2 in order that,

$$V_A = V_B \tag{2}$$

The voltages V_A and V_B are,

$$V_A = I_1 \cdot R_1 + V_{BE1} \tag{3}$$

$$V_B = V_{BE2} \tag{4}$$

The emitter area of the transistor Q_1 is N times greater than that of Q_2. Then from (1),

$$V_{BE1} = V_T \cdot \ln(I_1/N \cdot I_S) \tag{5}$$

$$V_{BE2} = V_T \cdot \ln(I_2/I_S) \tag{6}$$

As the transistors M_1 and M_2 are biased by the same gate-source voltage, they create the same drain current and therefore, $I_2 = I_1$. The difference of V_{BE} for the same current of the two bipolar transistors can be found by (5) and (6) as,

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = V_T \cdot \ln(N) \Rightarrow \Delta V_{BE} = \frac{\ln(N) \cdot k \cdot T}{q} \tag{7}$$

From (2)–(4),

$$I_1 = \frac{V_T \cdot \left(\ln\left(\frac{I_2}{I_S}\right) - \ln\left(\frac{I_1}{N \cdot I_S}\right) \right)}{R_1} \tag{8}$$

or

$$I_1 = \frac{V_T \cdot \ln(N)}{R_1} \tag{9}$$

So, I_1 ($= I_2$) is a PTAT current, proportional to ΔV_{BE} and it is created by transistors M_1, M_2 and M_3. Especially M_3 makes a copy of I_1 at the output node V_{ref}. It is obvious that the PTAT current depends on the transistors' area ratio N of Q_1 and Q_2. The resistor R_1 generates the difference in the emitter-base voltage between the two BJTs Q_1 and Q_2. The CTAT current is generated by OA2 and M_4. The current I_3 is suitably set in order that,

$$V_C = V_B \tag{10}$$

Since $V_B = V_A$,

$$V_C = I_1 \cdot R_1 + V_{BE1} = V_{BE2} = I_3 \cdot R_2 \tag{11}$$

From eq. (11) it is shown that $I_3 = V_{BE2}/R_2$ and as V_{BE} is CTAT then I_3 is CTAT. From (11) and (9),

$$I_3 = \frac{V_T \cdot \ln(N)}{R_2} + \frac{V_{BE1}}{R_2} \tag{12}$$

Considering that V_C must be close to V_B and V_A, without however the existence of a V_{BE} voltage, and for keeping R_2 at low value for a small layout, I_3 must be greater than I_1 by a factor of K. Summing proportionally the currents I_1 and I_3 a constant current is produced. However, the two currents are not equal and a gain factor must be applied to I_1. The total current must be temperature independent, meaning that,

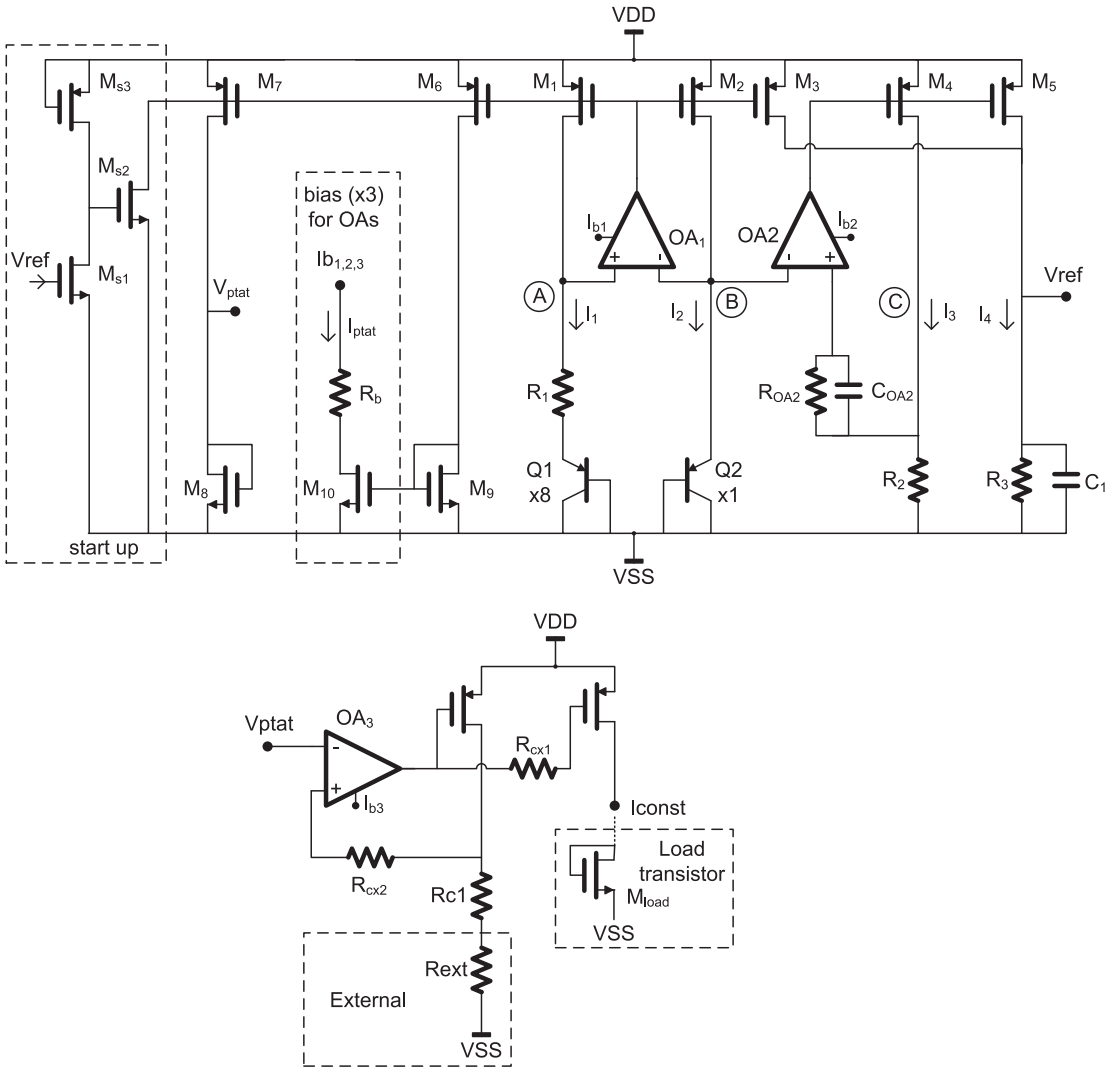

Fig. 2. The circuit of the constant voltage reference and the constant current generator.

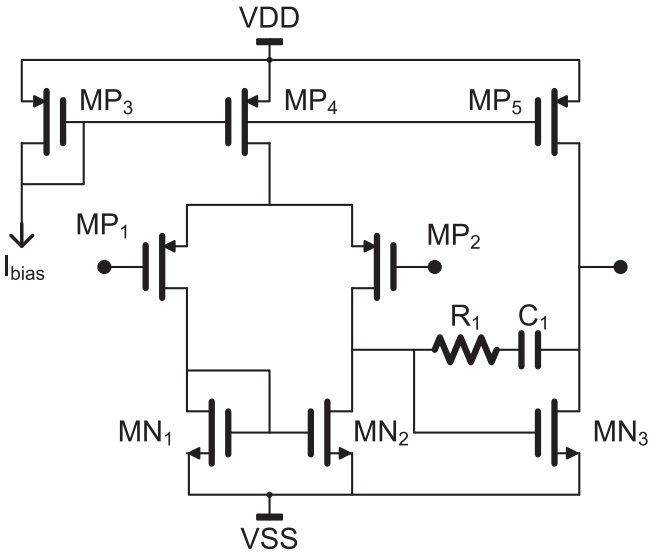

Fig. 3. The operational amplifier used in the voltage reference generator.

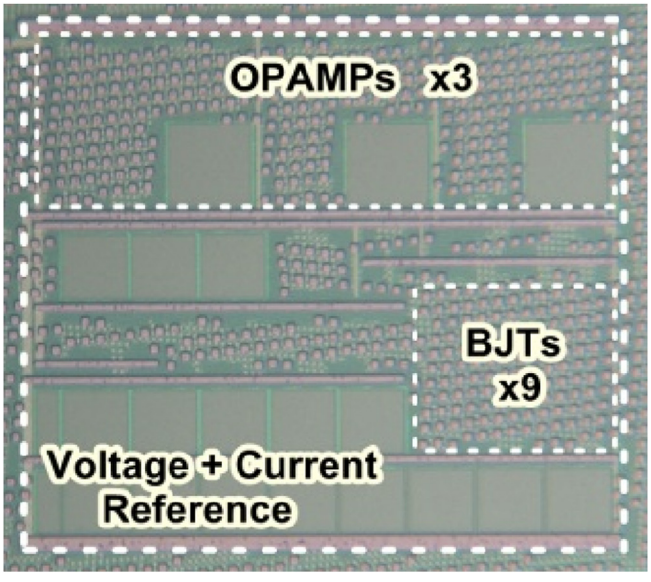

Fig. 4. Microphotograph of the BGR.

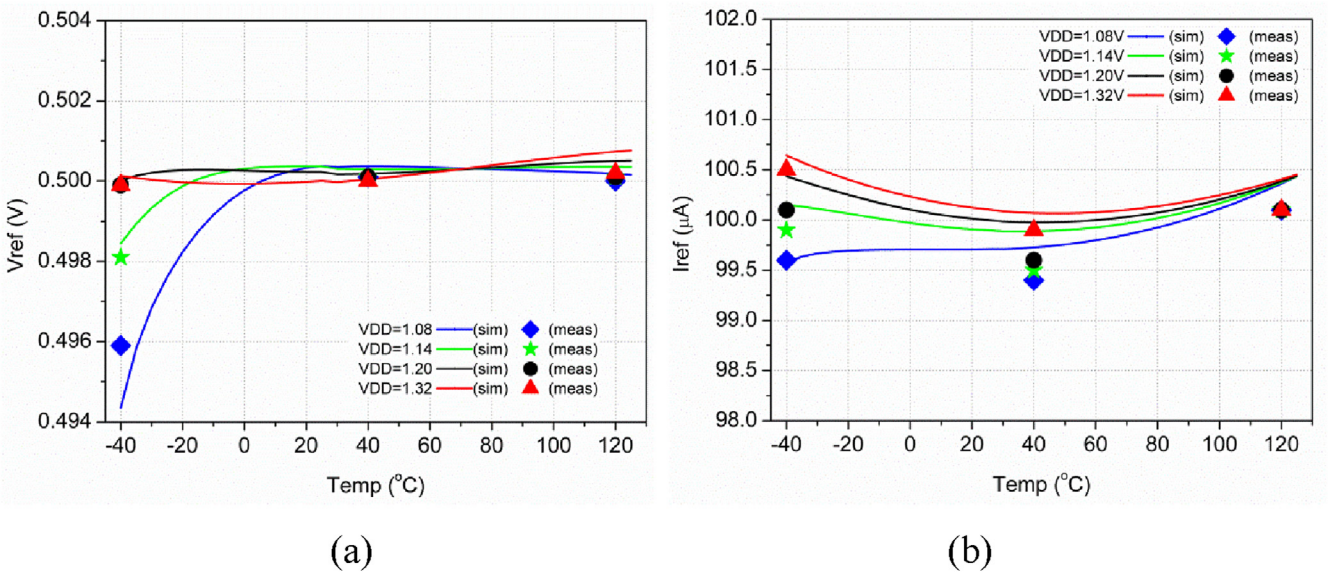

Fig. 5. Measurement results vs simulations over temperature and voltage variations a) voltage reference and b) current reference.

Table 1
Voltage reference generator and current reference performance.

Parameter	Conditions	Measurement
Technology	TSMC 65 nm LP	
V_{DD} (V)	Typical	1.2
Power (μA)	Typical @ 1.2 V, 27 °C	184
V_{ref} (mV)	Typical @ 27 °C, 1.2 V	500.1
ΔV_{ref} (mV)	Typical PV over ΔT[a]	499.9–500.1
ΔV_{ref} (mV)	Typical P over ΔT & ΔV[b]	500.2–495.9
ΔV_{ref} (mV)	PVT variations[c]	502.82–490.8
$\Delta V_{ref}/V_{ref}$ (%)	Typical PV over ΔT	0.04
$\Delta V_{ref}/V_{ref}$ (%)	Typical P over ΔT & ΔV	0.86
$\Delta V_{ref}/V_{ref}$ (%)	PVT variations[c]	2.40
I_{ref} (μA)	Typical @ 27 °C, 1.2 V	99.7
ΔI_{ref} (μA)	Typical PV over ΔT	100.1–99.6
ΔI_{ref} (μA)	Typical P over ΔT & ΔV	100.5–99.4
ΔI_{ref} (μA)	PVT variations[c]	102–98.5
$\Delta I_{ref}/I_{ref}$ (%)	Typical PV over ΔT	0.50
$\Delta I_{ref}/I_{ref}$ (%)	Typical P over ΔT & ΔV	1.1
$\Delta I_{ref}/I_{ref}$ (%)	PVT variations[c]	3.5
PSRR (dB)	Typical	−54
Noise (μV/√Hz)	Typical @ 100 Hz[c]	1.17

[a] ΔT in all cases is from −40 °C to 125 °C.
[b] $\Delta V = \pm 10\%$.
[c] Simulations.

$$\frac{\Delta}{\Delta T}(K\cdot I_1 + I_3) = 0 \Rightarrow \frac{\Delta}{\Delta T}\left(K\cdot\frac{V_T\cdot\ln(N)}{R_1} + \frac{V_T\cdot\ln(N)}{R_2} + \frac{V_{BE1}}{R_2}\right) = 0 \Rightarrow$$
$$K\cdot\frac{\ln(N)}{R_1}\cdot\frac{\Delta V_T}{\Delta T} + \frac{\ln(N)}{R_2}\cdot\frac{\Delta V_T}{\Delta T} + \frac{1}{R_2}\cdot\frac{\Delta V_{BE1}}{\Delta T} = 0 \Rightarrow \quad (13)$$
$$K = \left(-\frac{\Delta V_{BE1}}{\Delta T} - \frac{\Delta V_T}{\Delta T}\ln(N)\right)\cdot\left(\frac{\Delta V_T}{\Delta T}\right)^{-1}\cdot\frac{R_1}{R_2\cdot\ln(N)}$$

To keep the layout compact, the resistor R_3 at the output is relatively small. Then the final PTAT and CTAT currents are multiplied by a factor G in order to provide the desired value of V_{ref}, given by,

$$V_{ref} = (K\cdot I_1 + I_3)R_3\cdot G \Rightarrow$$
$$V_{ref} = K\cdot V_T\cdot\ln(N)\cdot\frac{R_3}{R_1}\cdot G + V_T\cdot\ln(N)\cdot\frac{R_3}{R_2}\cdot G + V_{BE1}\cdot\frac{R_3}{R_2}\cdot G \quad (14)$$

In order to solve (13) and (14), specific values are required in R_1, R_2, R_3, N. These values depend on the voltage generator requirements. A typical value for N is 8. This number is used to minimize the mismatch effect of the bipolar transistors. Setting an initial bias current equal to 1.5 (simulation 1.46) μA, taking into account that R_1 must be set at a suitable value in order that V_A to be close to V_B (650 mV) and from (9), then R_1 is calculated equal to 34.7 KΩ (used 37.3 KΩ). From (11), it is calculated $R_2 = 43.33$ KΩ (used 43.16 KΩ) to create a suitable current/voltage on node C. Solving (13), it results to $K = 8.7$. From (14) and for $G = 0.5$, the theoretical value of V_{ref} is 515 mV very close to the simulated, which is 501.5 mV at 27 °C.

3. Circuit design and considerations

A careful design was followed to provide better accuracy and better insensitivity of V_{ref} over PVT variations. The methodology followed, differentiate the proposed design from Ref. [28] and offer an improved performance:

a) All transistors have been designed with large length for better matching and reducing the short channel effect. The length of the PMOS transistors M_1 - M_7 is 3 μm, while the length of the NMOS transistors M_8 - M_{10} is 4 μm. The transistors of the startup sub-circuit are not critical and therefore the lengths are small.
b) All transistors of the BGR have large absolute dimensions. This way the mismatch effect is reduced in the expense of the layout area, which is increased. In addition, the large dimensions improve the power supply rejection ration (PSRR).
c) On the other hand, all resistors are designed with relatively low value, to keep the total layout within a limited area. The proper values have been chosen after a mathematical study as described in the previous section.
d) No large external capacitor is required for filtering or stability, used in other topologies. Only a small capacitor C_{OA2} is employed in the second opamp loop for stability and a small second internal capacitor $C_1 = 1$ pF at the output for noise filtering.
e) One critical point is the operational amplifier (opamp) used inside the voltage generators. Low dc offset and low drift opamp must be used. Using a simpler or more complex opamp is a tradeoff. A multi-stage operational amplifier offers improved performance, in terms of offset, gain and CMRR. On the other hand, a high gain amplifier may show instability issues in BGR needing additional stability compensation. Finally, the adjustment of the amplifier's operation within the loop may become harder than using a simpler opamp. A two-stage opamp may be more susceptible in dc offset, but its frequency

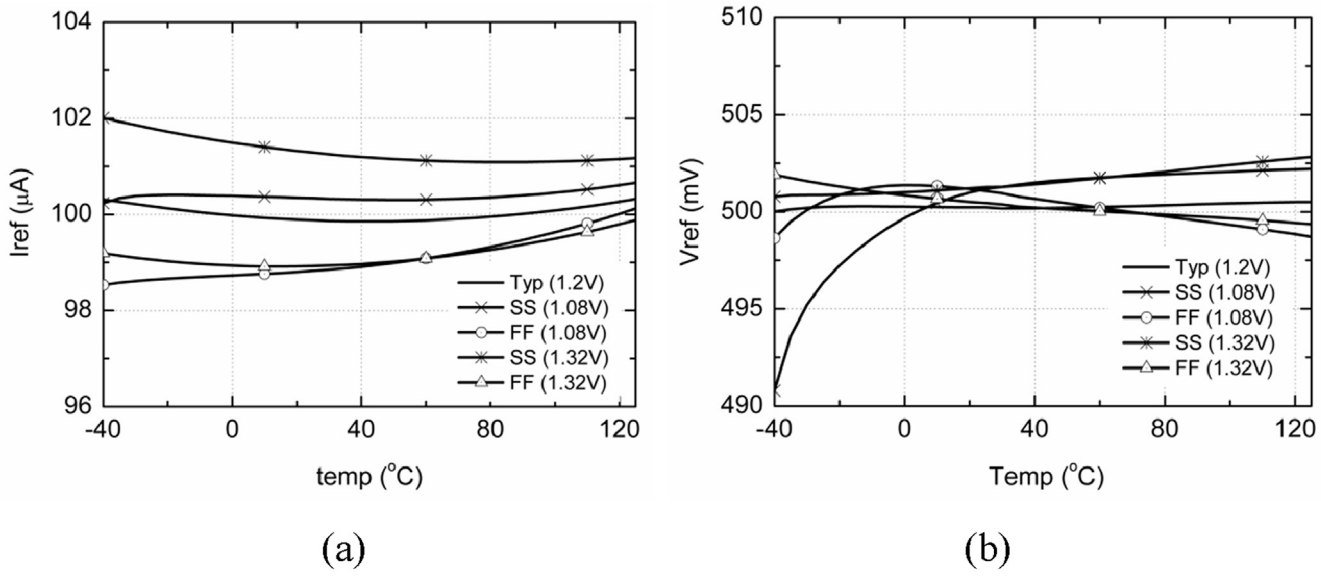

Fig. 6. Post-layout simulations results vs the temperature and supply voltage variations a) voltage reference and b) current reference.

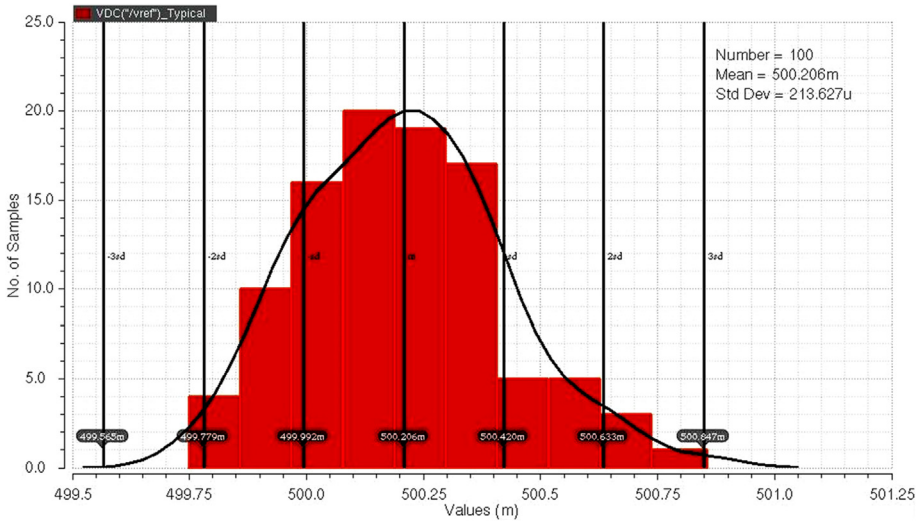

Fig. 7. Simulated post-layout monte-carlo results of the voltage reference *Vref*.

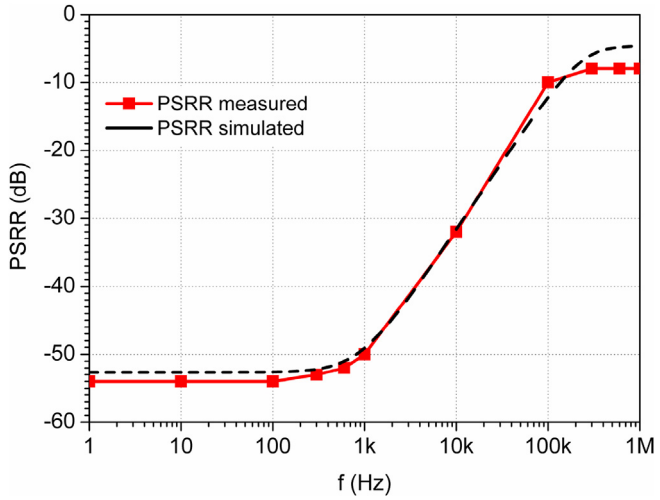

Fig. 8. PSRR a) measured, b) simulated.

compensation may be easier. In our design, a simple two-stage opamp has been chosen which is biased by a PTAT current to compensate the output drift.

The opamp circuit is based on a simple topology as shown in Fig. 3. The differential pair is constructed by PMOS transistors and the second stage is constructed by the NMOS transistor MN_3. This structure suits better with the input voltage range and additionally, the output is better driving the PMOS transistors of the voltage generator, which are connected at the output. A rail-to-rail opamp could be used instead, to improve accuracy of the reference voltage, especially at the low temperature corner. However, the small improvement of the accuracy would be worthless taking into account the increased power and layout area consumption. Therefore, a carefully designed conventional opamp, taking into account the input and output voltage range, is sufficient. As shown in Fig. 2, the bias current is received by the PTAT current internally generated by the voltage reference generator.

A typical circuit, consisting by MS_1, MS_2 and MS_3, is employed to ensure the proper startup operation.

Table 2
Comparison with other fabricated BGRs.

	This work	[4]	[5]	[6]	[8]	[10]	[15]	[16]	[17]	[19]	[20]	[21]	[22]	[24]	[25]	[26]	[28] [a]	[29]	[31]
Process	65 nm	0.8 μm	0.5 μm	0.5 μm	0.4 μm	1.2 μm	0.18 μm	130 nm	0.35 μm	0.35 μm	0.13 μm	180 nm	180 nm	0.5 μm	0.18	0.18 μm	90 nm	0.35 μm	180 nm
VDD (V)	1.2	1	–	1	–	1.2	–	–	–	–	0.6	0.5		1	–	0.75	1	1	>1.5
VDD range (V)	1.08–1.32	>0.95	1–5	1–5	>0.84		>0.65	1–3.3	>0.95	1.5–4.3	0.6–1.8	0.5–0.9	0.55–1	0.95–3.3	0.7–1.8	0.65–1.8	0.9–1.1	0.9–1.6	1–2.5
ΔT (°C)	−40–125	0–80	−40–125	−40–125	27–125	−25–125	0–120	−40–85	−20–80	0–80	−25–80	−25–80	−45–140	−40–125	−32–125	−60–130	−36–125	−20–50	−40–140
Vref (mV)	500	536	190.9	190.9	518	295	192	598	741	168	499.8	240	460	–	0.32	0.323	510	0.75	500
$\Delta V_{ref}/V_{ref}$ (%) (T variation)	0.04	0.06	–	–	–	–	–	0.6	0.4	0.0025	0.083	0.35	0.54	–	0.23	0.91	0.39	–	0.57
$\Delta V_{ref}/V_{ref}$ (%) (VT variation)	0.86	–	1.14	1.14	1.14	7.3	1	–	–	–	–	–	–	0.47	–	9	–	>1.8	–
Idd(μA)	155	–	27	20	2.2	–	0.6	1 @ 1 V	0.250	2	0.622	–		–	–	5.33	208	10	–
Power consum. (μW)	186	–	–	–	–	–	0.39	–	0.390	–	0.373	0.04	0.083	–	2.7	4	208	–	–
Area (mm^2)	0.04	3	–	–	0.1	0.23	0.08	0.02	0.076	0.08	0.036	0.058	0.061	1.09	0.023	0.039	0.049	–	–
PSRR (dB) @100 Hz	−54	–		–	–	−40 @ 10 KHz	−52.5	−44	−23.7 @ 1 KHz	−65	−80	−62	−62 [a]	–	−28		−52.78	40	–
Noise @100 Hz (μV/√Hz)	1.16	–	40 @ 1 KHz	0.04	–									–	59 μV (1–50 Hz)	45 μV (1–50 Hz)	257 μV (1-1 GHz)	180 μV (10-1 MHz	0.205 @ 100 KHz
Mismatch(σ/μ %)	0.043 [a]	–	0.19	0.19	0.98	–	0.27	–	–	–	1.38	0.76	0.8	–	–	–	0.88 [b]	–	–

[a] Simulation.
[b] 3 voltages and 3 temperatures.

4. Simulation results and chip measurements

The BGR presented so far has been designed and fabricated on the TSMC 65-nm 1P9M CMOS MS/RF low power (LP) process optimized for low leakage currents. The die area is 215 μm x 242 μm for both the voltage and the current generator excluding the pads; the area of the voltage generator standalone only is 0.04 mm^2. The microphotograph of the fabricated die is shown in Fig. 4. The bare die has been wire-bonded to a board (chip-on-board, CoB). The results were obtained by using an Agilent 34401A digital multimeter under the environment provided by the Tenney TJR temperature test chamber.

A number of operating conditions in terms of supply voltage and temperature have been applied to evaluate the circuit performance. The nominal operating supply voltage V_{DD} is 1.2 V, the nominal generated reference voltage is 500.1 mV and the nominal reference current is 100 μA. Measurement results show V_{ref} value equal to 500.1 mV at 25 °C and a variation of 0.04% over a temperature (T) range from −40 °C to 125 °C. For the same temperature range, together with ±10% V_{DD} (V) variation, the output voltage is varied within a range of 0.86% overall, as shown in Fig. 5a. Measurement and simulation results are, both depicted in Fig. 5a allowing them to be easily compared. It is shown that the performance of the fabricated chip is well predicted by the simulations. The detailed measurement results are summarized in Table 1.

On the same die, a constant current generator has been included, with a nominal current of 100 μA. Measurement of the reference current at the typical PVT case gives a value of 99.7 μA. As shown in Fig. 5b a small systematic error exists in the measurements, explained by the tolerance of the external reference resistor. The current variation over ±10% voltage variation and over a temperature range from −40 to 125 °C is only 1.1%.

The performance over process corners has not been evaluated because the required large number of fabricated chips from different tape-out runs was not available. Instead, post-layout simulations have been performed under corner conditions and the results are shown in Fig. 6. It is shown that even under process, voltage and temperature (PVT) variations, the final variation of V_{ref} remains very low, around 2.5% and of I_{ref} about 3.5%. Post-layout monte-carlo mismatch simulations have been performed and the results showed a mean value m = 500.2 mV and a standard deviation σ = 213 μV, as depicted in Fig. 7. This corresponds to a percentage variation σ/m = 0.043%. The output noise is 1.17 $\mu V/\sqrt{Hz}$ at 100 Hz, while the integrated noise is 24.4 μV for the frequency range from 1 Hz to 100 Hz. The cost paid for the good mismatch performance and the low noise is the high power consumption.

The Power Supply Rejection Ratio (PSRR) was measured to be −54 dB at 100 Hz. The measured PSRR vs the frequency plot is very close to the simulated one, as depicted in Fig. 8. The response is exactly as it was expected from the defined specifications of our application and the fact that the PSRR worsens in higher frequencies does not affect our system performance. The typical startup time with V_{DD} equal to 1.2 V and temperature 27 °C is less than 2 μs. The worst-case startup time is 6 μs when V_{DD} is 1.08 V and temperature −40 °C.

A comparison with other fabricated chips providing with voltage references below 1 V is summarized in Table 2. It is shown that the proposed voltage generator provides a V_{ref} with the smallest variation over supply voltage and temperature variation. For the measurement, the supply voltage was set 1.2 V ± 10% over temperature range from −40 °C to 125 °C. The total V_{ref} variation is only 0.86%. Comparing with a similar subthreshold circuit [28] the proposed circuit has the following benefits: a) simpler, not rail-to-rail) opamps, b) smaller area, c) better layout placement of critical bipolar transistors d) smaller current and power consumption, e) no need for external output capacitors and f) most important, better accuracy and stability. Although some of the reference voltage generators show a low sensitivity [4,27,31,32], the results presented are under constant supply voltage with only temperature variation. Testing our circuit over temperature variation only and keeping V_{DD} constant, it gives V_{ref} variation of only 0.04%, still better than the

compared topologies. In addition, it shows a very competitive performance in terms of output voltage invariance, comparing with some low power voltage generators [4,8,14–20,29] which they operate and have been tested in much smaller temperature range. The topology in Ref. [15] requires a clock and the generators in Refs. [25,26] operating in subthreshold with low power consumption and wide temperature range, need additional trimming after fabrication in order to exhibit a good performance. Works in Refs. [21] and [22] employ low voltage, low power topologies based on weak inversion operation. They use internal V_{DD} doubler, clocked switched-capacitor V_{BE} divider, and buffer to drive high load currents, increasing the total power consumption.

In an overall comparison with the other implementations shown in Table 2, the proposed voltage generator shows the best performance in terms of V_{ref} accuracy, the lowest noise after that in Ref. [6], and the lowest mismatch effect. The main drawback is the increased power consumption. However, the increased consumption allows for using smaller passive resistors, resulting smaller layout area, while offering a high driving capability able to drive almost any load in a system. Finally, the PSRR is comparable with the other implementations presented in Table 2. The overall performance of the proposed circuit makes it suitable for many applications requiring an accurate and reliable constant voltage generator.

5. Conclusions

A voltage reference generator is proposed in this paper, targeting to a design with low sensitivity over supply voltage and temperature variation. A detailed theoretical analysis is provided and the performance is verified through simulations and measurements. The circuit was fabricated in a 65 nm LP process. Measurements of the fabricated chip show a constant reference voltage equal to 500.1 mV under a typical supply voltage of 1.2 V. The output voltage variation is less than 0.9% within a temperature range from −40 to 125 °C together with a supply voltage variation of 1.2 V ± 10%. Additionally, the circuit requires a small layout area and shows a good noise performance. A constant current reference generator has been fabricated as well and a constant current of 100 μA was measured with variation of about 1%.

References

[1] R.J. Widlar, New development in IC voltage regulator, IEEE J. Solid State Circ. 6 (1971) 2–7.

[2] C. Yao, B. Liu, Y. Xia, A 14-/spl mu/A 3-ppm//spl deg/C CMOS bandgap voltage reference, in: 2005 6th International Conference on ASIC, 2005, pp. 503–506, https://doi.org/10.1109/ICASIC.2005.1611366.

[3] Y. Dai, D.T. Comer, D.J. Comer, C.S. Petrie, Threshold voltage based CMOS voltage reference, IEE Proc. Circ. Dev. Syst. 151 (2004) 58–62.

[4] P. Malcovati, F. Maloberti, M. Pruzzi, C. Fiocchi, Curvature compensated BiCMOS bandgap with 1V supply voltage, in: ESSCIRC, 2000, pp. 7–10.

[5] V.V. Ivanov, K.E. Sanborn, I.M. Filanovfsky, Bandgap voltage references with 1V supply, in: ESSCIRC, 2006, pp. 311–314.

[6] K. Sanborn, M. Dongsheng, V.V. Ivanov, A sub-1-V low noise bandgap voltage reference, IEEE J. Solid State Circ. 42 (2007) 2466–2481.

[7] A. Annema, Low-power bandgap references featuring DTMOST's, IEEE J. Solid State Circ. 34 (1999) 949–955.

[8] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, K. Sakui, A CMOS bandgap reference circuit with sub-1-V operation, IEEE J. Solid State Circ. 34 (1999) 670–674.

[9] J. Ma, Y. Li, C. Zhang, Z. Wang, A 1V Ultra-low Power High Precision CMOS Voltage Reference, EDSSC, 2007, pp. 847–850.

[10] G. Giustolisi, G. Palumo, M. Criscione, F. Cutri, A low-voltage low-power voltage reference based on subthreshold MOSFETS, IEEE J. Solid State Circ. 38 (2003) 151–154.

[11] I. Nissinen, J. Kostamovaara, A low voltage CMOS constant current–voltage reference circuit, ISCAS 1 (2004). I-381–I-384.

[12] S. Miller, L. MacEachern, A Nanowatt Bandgap Voltage Reference for Ultra-low Power Applications, ISCAS, 2006, pp. 645–648.

[13] S. Koudounas, J. Georgiou, Reduced-area, Low-power CMOS Bandgap Reference Circuit, ISCAS, 2007, pp. 3832–3835.

[14] Y. Zeng, Y. Huang, Y. Luo, H.Z. Tan, An ultra-low-power CMOS voltage reference generator based on body bias technique, Microelectron. J. 44 (2013) 1145–1153.

[15] P.B. Basyurt, E. Bonizzoni, D.Y. Aksin, F. Maloberti, Voltage reference architectures for low-supply-voltage low-power applications, Microelectron. J. 46 (2015) 1012–1019.

[16] A. Parisia, A. Finocchiarob, G. Palmisano, An accurate 1-V threshold voltage reference for ultra-low power applications, Microelectron. J. 63 (2017) 155–159.

[17] L.H.C. Ferreira, T.C. Pimenta, R.L. Moreno, A CMOS threshold voltage reference source for very-low-voltage applications, Microelectron. J. 39 (2008) 1867–1873.

[18] L. Xinquan, X. Ziyou, L. Yanming, Y. Qiang, M. Maoli, A CMOS piecewise curvature-compensated voltage reference, Microelectron. J. 40 (2009) 39–45.

[19] G.D. Vita, G. Iannaccone, Ultra-low-power temperature compensated voltage reference generator, Microelectron. J. 37 (2006) 1072–1079.

[20] L. Liu, Y. Song, J. Mu, W. Guo, Z. Zhu, Y. Yang, A high accuracy CMOS subthreshold voltage reference with offset cancellation and thermal compensation, Microelectron. J. 60 (2017) 102–108.

[21] J. Mu, L. Liu, Z. Zhu, Y. Yang, A 58-ppm/◦C 40-nW BGR at supply from 0.5 V for energy harvesting IoT devices, IEEE Trans. Circ. Systems II: Expr. Briefs 64 (2017) 752–756.

[22] L. Liu, J. Mu, Z. Zhu, A 0.55-V, 28-ppm/°C, 83-nW CMOS sub-BGR with ultra low power curvature compensation, IEEE Trans. Circ. Syst. Regular Pap. 65 (2018) 95–106.

[23] A. Tajalli, Y. Leblebici, Subthreshold MOS for Ultra-low Power, in: Extreme Low-power Mixed Signal IC Design: Subthreshold Source-coupled Circuits, Springer New York, New York, NY, 2010, pp. 15–58, https://doi.org/10.1007/978-1-4419-6478-6_2 isbn=978-1-4419-6478-6.

[24] J. Doyle, J.L. Young, B.K. Yong, H. Wilsch, F. Lombardi, A CMOS subbandgap reference circuit with 1-V power supply voltage, IEEE J. Solid State Circ. 39 (2004) 252–255.

[25] C.M. Andreou, J. Georgiou, A 0.7 V, 2.7 μW, 12.9 ppm/° C over 180° C CMOS subthreshold voltage reference, Int. J. Circ. Theor. Appl. 45 (2017) 1349–1368, https://doi.org/10.1002/cta.2292.

[26] C.M. Andreou, J. Georgiou, A 0.75-V, 4-μW, 15-ppm/°C, 190 °C temperature range, voltage reference, Int. J. Circ. Theor. Appl. 44 (2016) 1029–1038, https://doi.org/10.1002/cta.2122.

[27] M. Jingwen, C. Tingqian, C. Cheng, R. Junyan, Y. Li, CMOS 1.5V bandgap voltage reference, ASICON 1 (2005) 469–472.

[28] A. Tsitouras, F. Plessas, M. Birbas, J. Kikidis, G. Kalivas, A sub-1V supply CMOS voltage reference generator, Int. J. Circ. Theor. Appl. 40 8 (2012) 745–758.

[29] K. Lasanen, V. Korkala, E. Raisanen-Ruotsalainen, J. Kostamovaara, Design of a 1-V low power CMOS bandgap reference based on resistive subdivision, MWSCAS 3 (2002) 564–567.

[30] P.K.T. Mok, K.N. Leung, Design Considerations of Recent Advanced Low-voltage Low-temperature-coefficient CMOS Bandgap Voltage Reference, CICC, 2004, pp. 635–642.

[31] A. Boni, Op-amps and startup circuits for CMOS bandgap references with near 1-V supply, IEEE J. Solid State Circ. 37 (2002) 1339–1343.

[32] I.M. Filanovsky, A. Allam, Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits, IEEE Trans. Circ. Syst. Fund. Theor. Appl. 48 (2001) 876–884.