A 76–84 GHz CMOS 4× Subharmonic Mixer With Internal Phase Correction

Fotis Plessas, *Senior Member, IEEE*, George Souliotis, *Member, IEEE*, and Rodoula Makri, *Member, IEEE*

***Abstract*— A CMOS 4× subharmonic mixer (SHM) with an internal phase error correction mechanism operating at mm-wave frequencies is proposed in this paper. The SHM operates with a 81-GHz RF input signal and a 20-GHz local oscillator (LO) signal to produce a 1-GHz output. The single ended input is converted into octet-phase, through an active input balun, an active polyphase filter, and certain phase adders. A phase calibration technique is employed, to compensate the phase deviations due to the circuit mismatches, offering a ±5° phase adjustment between the generated phase shifts. By this technique, a close to optimal performance can be obtained, especially in terms of conversion gain and LO-IF isolation, which can be improved by 1.5 to 7.5 dB and by 5 to 17 dB, respectively. Fabricated in a 65-nm CMOS low-power technology, the prototype exhibits a conversion gain of −8 dB (without using an IF amplifier), a 1 dB compression point (P_{1dB}) of −10 dBm, a third-order intercept point (IIP3) of 1 dBm, and a noise figure of 15 dB. The power consumption is 213 mW, and port-to-port isolation is >70 dB. The achieved performance compares well with the state of the art at these high frequencies despite the use of a slower CMOS process.**

***Index Terms*— mm-wave frequencies, mixers, phase adders, subharmonic, radio frequency integrated circuits.**

I. Introduction

MILLIMETER wave communications systems are evolving rapidly in recent years. The use of millimeter wave (mm-wave) frequencies is given particular attention nowadays, especially when considering the increased requirements for bandwidth and data traffic volumes. Since the demand for broadband services grows immensely while moving to 5G, wireless communications need to support high data rates which, in turn, dictates the use of mm-wave systems, even at the first half of IEEE W-band (75-110 GHz), at the lowest possible cost and with the highest integration.

Designing receivers for such systems, where the operation frequencies are in the range of tens of GHz, presents quite many challenges, particularly when considering chip implementations. A most important challenge is related to the design difficulties of the local oscillators (LO) in these high frequencies, especially in standard CMOS technologies. The direct-conversion technique seems attractive in these cases since it converts the RF signal to Baseband, without the need of bulky filters; thus, imposing the use of high frequency oscillators. However, the direct-conversion mixers suffer from the self-mixing DC offset [1], causing decreased performance. The DC offset is generated from the LO's strong signal which, due to coupling, returns to the mixer from the RF signal path.

A suggested technique is to use a lower frequency LO by employing a subharmonic mixer (SHM). SHMs need LO operating in one-half or, even better, in one-quarter of the required frequency, solving by this way the problem of the self-mixing DC offset [1]. Furthermore, apart from direct-conversion, SHMs can be also used in heterodyne-type receivers as well as any other mixer application. Especially at mm-wave frequencies the reduction of the local oscillator frequency by a factor of two or four is beneficial, simplifying the LO design and improving the phase noise performance.

Although SHMs need a lower LO frequency, they use internally generated higher harmonics to perform the mixing with the RF signal. SHMs using LO with *one—half* the frequency that would be required for a fundamental-mode have been developed in the frequency range from 1GHz to 5GHz [3]–[8]. A SHM operating in 50 GHz is presented in [9], implemented in a SiGE BiCMOS technology. To make the design easier for GHz receivers, 4× SHMs have been proposed [10]–[13]. They only need a quarter of the frequency required by a typical non-subharmonic mixer. The produced IF frequency in that case is,

$$f_{IF} = f_{RF} - 4 \cdot f_{LO}. \tag{1}$$

However, the drawback in this technique is that an octet-phase LO signal is required. With the use of phase adders, the differential LO signal should be converted initially to signals with 0°, 90°, 180° and 270° relative phase shifts and then to those with phase shifts of 45°, 135°, 225° and 315°. Although simple RC networks can be used as passive phase adders, they are inherently susceptible to process variations and the output signal may be significantly attenuated. On the contrary,

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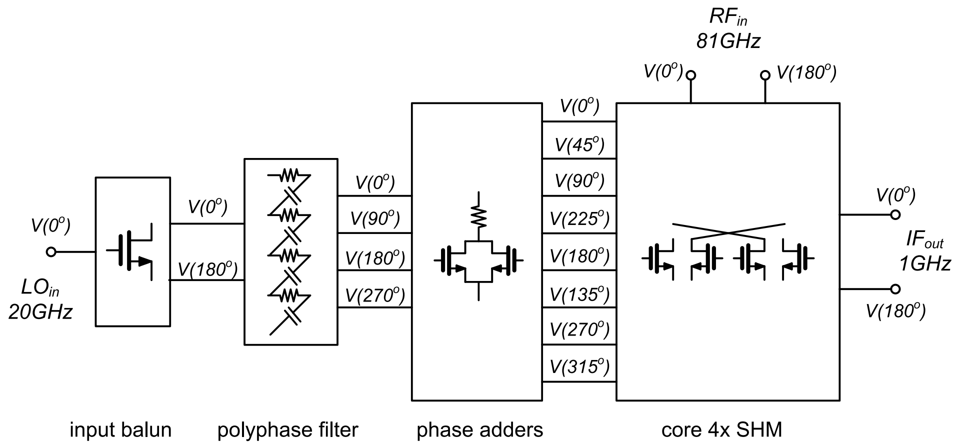

Fig. 1. The block-diagram of the 4× subharmonic mixer.

active phase adders are less sensitive to process variations and offer improved performance. However, they still suffer from mismatches, which reduce the accuracy in the produced signal phases and they degrade the overall performance of the mixer.

Generally, any mismatch between the eight phase shifts needed, can affect the total conversion gain and quality of the output signal. The core of the mixer is also sensitive to process, voltage and temperature (PVT) variations. Mismatches in the device physical dimensions can deteriorate the linearity (second-order inter-modulation distortion).

Driven from the above, in this paper, a 76-84 GHz 4× subharmonic mixer with internal phase compensation of the LO phases is proposed. It will be shown that the overall performance is significantly improved by including a novel compensation technique to correct the phase errors produced by the mismatches in the phase adders used before the mixer. Moreover, active phase adders for all phases have been used, offering improved accuracy and gain. Differing from other similar cases, the body-voltage of specific nMOS and pMOS devices at the polyphaser filters can be externally controlled to forward-bias their body-to-source terminals. Leveraging forward body biasing (FBB), we can speed-up the circuit when it is slower than nominal due to process, voltage and temperature variations.

At this point it should be noted that the circuit is designed in a 65-nm Low Power (LP) CMOS process with 1.2 V supply voltage. 65-nm LP n-MOSFETs exhibit lower transconductance than General Purpose (GP) devices at comparable physical gate length; thus, the decision to select LP CMOS for mm-wave applications is not beneficial for achieving large f_T, f_{MAX} and low noise figure, as often needed in 80-100 GHz ICs. However, it would be challenging to evaluate the proposed architecture and implementation in a LP technology node, offering devices with degraded analog/RF performance, pushing in this way the limits of the node with respect to the demanding specifications of backhaul and broadband applications. To the best of the authors' knowledge, this is the first 4× subharmonic mixer in mm-wave frequencies, designed using an LP process and featuring phase adjustment and forward-body bias to improve performance.

This paper is organized as follows: Section II addresses the mixer circuit design and analysis, Section III reports the implementation and experimental results, and the conclusion is drawn in Section IV.

II. Circuit Design

The circuit under examination has been designed in a CMOS LP technology node. This process is optimized for digital designs and is rather unsuitable for demanding, high speed mm-wave circuits. The performance of the devices makes the design too challenging, especially for the mm-wave circuits, where the transconductance should remain high. On the other hand, it should be also considered that most on-chip complete system designs and implementations are digital in a large degree. Therefore, it is equally important to test the possibility of placing together on a single die, a mm-wave circuit and a digital design which is mainly used for control or for post-processing of lower frequency signals. Therefore, the subharmonic mixer of the present work has been implemented and fabricated on an LP process.

The topology of the 4× SHM is shown in the block diagram of Fig.1. The RF signal (RF_{in}) is differential at 81 GHz, the LO signal (LO_{in}) is single ended at 20 GHz and consequently, the IF output (IF_{out}) is at 1 GHz. The core of the 4× SHM requires octet-phase LO signals (i.e. 0°, 45°, 90°, 135°), 180°, 225°, 270°, and 315°, as shown in Fig.2, generated by the preceding stages from a single ended LO signal LO_{in}. The first stage is an active balun [8], the second stage is a polyphase filter and the third one is a phase adder. The balun converts the single ended LO_{in} into differential output (0° and 180°). The relevant circuitry consists of two transistors, as shown in Fig.3. The two output phases 0° and 180° of the balun are used to generate all the other phases. At first, a polyphase filter generates a quadrature output signal with phases of 0°, 90°, 180° and 270°.

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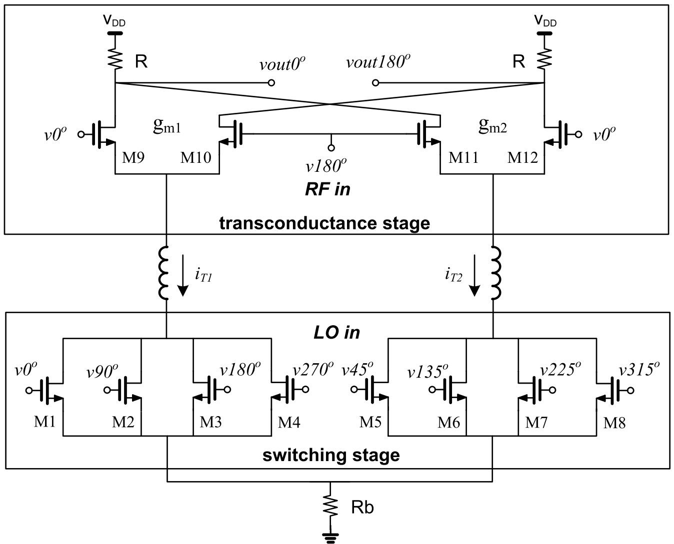

Fig. 2. The topology of the 4× subharmonic mixer core [11].

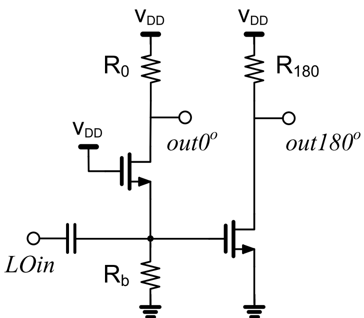

Fig. 3. The active balun.

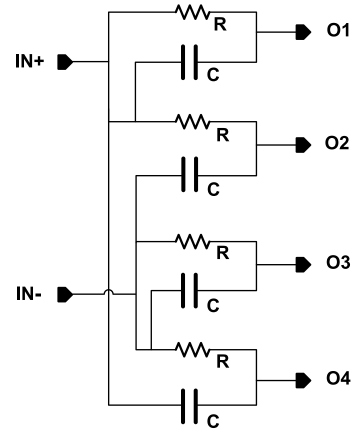

Fig. 4. A typical Passive polyphase filter.

phases of 0°, 90°, 180° and 270°. Four 45° phase adders use phase pairs with 90° difference in respect to the signals generated by the first phase adder, to produce the intermediate phases of 45°, 135°, 225° and 315°. Then, all eight phases from 0° to 315° with 45° phase difference are made available for the core of the 4× SHM.A 0° phase adder is also used to match the delays between the 0°, 90°, 180° and 270° phases with those of 45°, 135°, 225° and 315° phases. This is similar with the 45° phase adder, but the two inputs receive the same phase of 0°, 90°, 180° or 270°. Furthermore, the 0° phase adder includes a different valued termination resistor for amplitude compensation; otherwise the amplitude would be $\sqrt{2}$ times greater than that of the 45° phase adder [10].

A. The Polyphase Filter

The simplest method to create four phases from a differential signal is by means of a passive polyphase filter. A single-stage passive polyphase filter is depicted in Fig.4. This method suffers from process tolerances and mismatches, that may result in phase errors along with output attenuation [10], [11], [14]. An additional important issue by using passive RC 90° phase adders is that the components tolerance in the fabrication process can lead to a larger phase and amplitude errors than those showed in simulations and the resulting mixer performance could be degraded [11]. A detailed analysis of passive polyphase filters is given in [15] where high losses are shown. Passive polyphase filters with additional stages may improve the phase error; however, due to the attenuation at the multiple stages, several gain buffers should be used. Active polyphase filters may offer higher gain, less sensitivity in process variations [10], ability for tuning [16] and better isolation between stages.

In this work, an active polyphase filter has been utilized, which offers better gain, better phase matching, and satisfactory isolation towards the next blocks [17]. The active polyphase filter, shown in Fig.5, consists of four stages in cascade configuration while all stages are based on inverters. Although the basic gain circuit could be an operational transconductance amplifier, the employment of a much simpler inverter offers the desired ability for operation at higher frequencies. The first two stages form the core of the polyphase filter and they generate four phases with 90° phase difference to each other. Even though an active polyphase filter could be made by one stage, two stages significantly improve the phase error.

The inverter based polyphase filters have been realized in [18] and [14]. A detailed analysis, considering the active polyphase filter implemented with transconductors, and the non-idealities, is given in [16]. Also, in [15] the passive muti-stage polyphase filter is extensively studied including all parasitic effects and gain losses. The simplified transfer function of the first stage of the polyphase filter (Fig.5) is given by [16]:

$$\frac{I_{I1}}{Vin} = \frac{1+\tau s}{\tau s} \tag{2}$$

$$\frac{I_{Q2}}{Vin} = \frac{1-\tau s}{\tau s} \tag{3}$$

where, $I_{I1} = I_{I1p} - I_{I1n}$ is the differential output current of the I output, I_{Q1}=$I_{Q1p} - I_{Q1n}$ is the differential output current of the Q output, $V_{in} = V_{in0} - V_{in180}$ is the differential voltage input, and τ is the time constant. If the dominant factor of the first stage is the transconductance g_{m1}, then $\tau = C/g_{m1}$.

The last two stages, consisting of inverters, are used to provide the necessary isolation and gain. The basic element of all active stages of the above circuits is a simple CMOS inverter; where the Cherry-Hooper technique [19] has been

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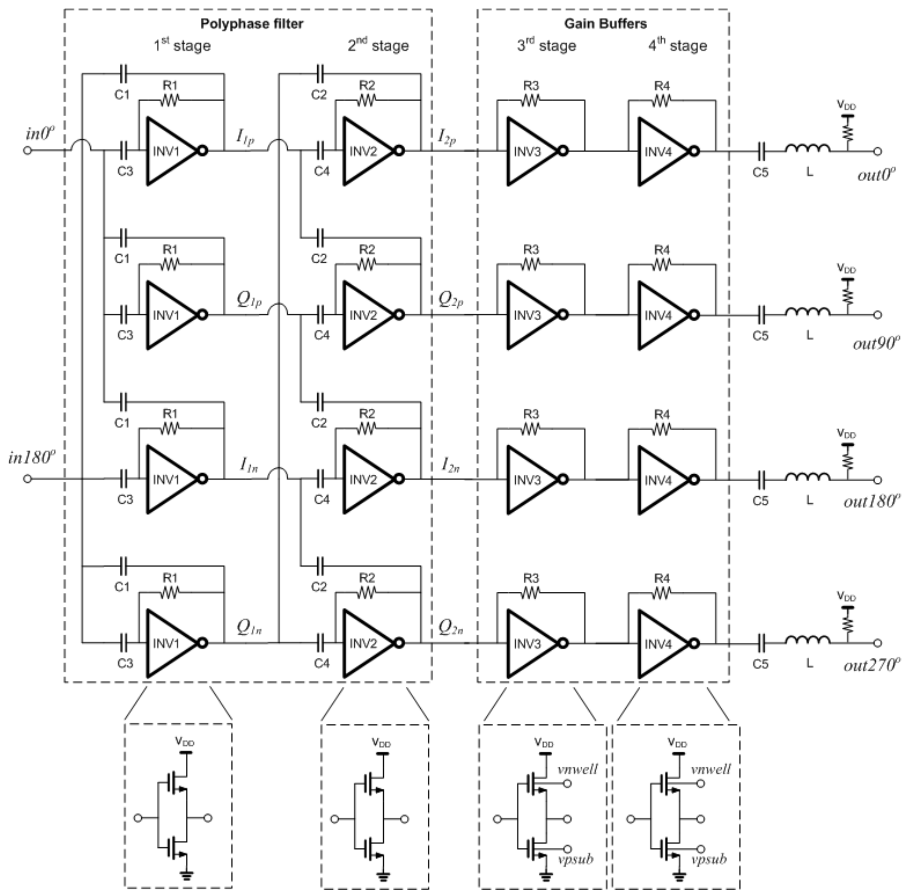

Fig. 5. The proposed schematic for the active polyphase filter.

applied with a feedback resistor from the output to the input, so that to improve the circuits' bandwidth.

As the output impedance of the 2nd stage is high, additional buffering stage must be added at the filter's output [16]. Extra gain stages are also required to improve the total gain thus; the last two inverters are used as gain buffers.

The body terminals of the p-MOS and n-MOS transistors at the last two inverters are not connected to the supply voltage and ground respectively, but to external pins; one for the body terminals of the p-MOS devices and one for the body terminals of the n-MOS devices. Thus, a forward body biasing (FBB) technique is applied, suitably, for post-silicon tuning [20], [21]. By utilizing this technique, the threshold voltage decreases resulting in drain current increase, which in turn improves the speed of the circuit at the expense of a moderate increase in leakage power. FBB methodology works on the principle of applying a positive voltage v_{bs} to the body terminal of the NMOS transistor and a positive voltage of $VDD - v_{bs}$ to the PMOS transistor. The limitation however is that the forward bias must be small enough to prevent the junction diodes from being turned on. This forces the forward bias range to be below the PN diode built-in potential, providing an acceptable range of about 500 mV. It should be noted that an extensive simulation-based study was carried out, indicating that unlike the rest of the blocks, the most significant improvement occurs when FBB is applied to the polyphase filter improving the gain at PVT corners.

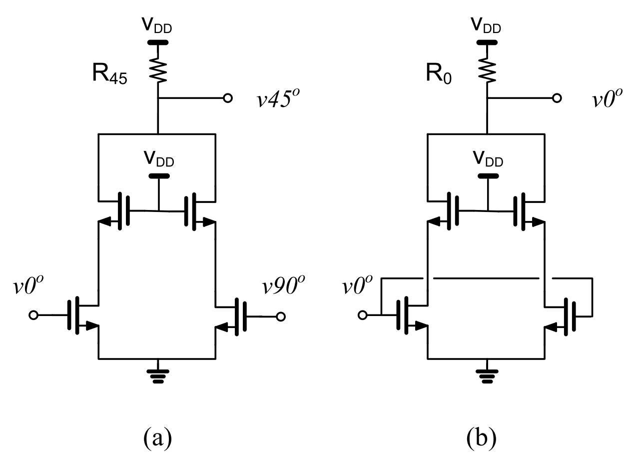

Fig. 6. 45° phase adder (a) and 0° phase adder (b).

B. Phase Adder With Phase Control

A 45° phase shifted signal can be generated by adding two signals with a 90° phase difference to each other. The simplest way to create a relative phase shift of 45° is by using passive RC-CR networks, facing, however, the problems described already in the previous paragraph. Another way to generate a 45° signal is by using an active adder [6], [10], [11] as shown in Fig.6. The behavior of a phase adder can be also described based on phase interpolator circuits [22]. This particularly helps in explaining the operation of the proposed circuit. The principle of phase generation by a current mode

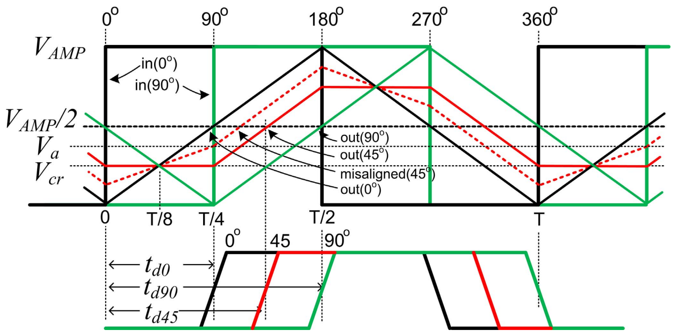

Fig. 7. Waveforms of phase adders.

phase interpolator is to add two currents of the same weight but with 90° phase difference, expressed as,

$$A \cdot \cos(\omega t) + A \cdot \cos(\omega t + \pi/2) = \mathrm{A}\sqrt{2}\cdot\cos(\omega t + \pi/4) \quad (4)$$

The resulting current is transformed into voltage through resistor R_{45} as shown in Fig.6(a). A 0° phase adder is also used, for each one of the 0°, 90°, 180°, or 270° signals, to match the delay with that of the 45° signal. This is actually a delay element, providing a delay equal to that of the 45° phase adder. In this case, the two inputs are connected together thus,

$$A \cdot \cos(\omega t) + A \cdot \cos(\omega t) = 2\cdot A \cdot \cos(\omega t) \quad (5)$$

From (4) and (5) it is derived that the amplitude is different between the two phase adders. This can be corrected by properly adjusting the resistors R_0 of the in-phase adder and R_{45} of the 45° phase adder shown in Fig.6(b). The ratio between the resistors will be $R_{45} = R_0\sqrt{2}$.

Even with the active adders, phase errors may occur as well due to transistor mismatches, parasitic capacitances, non-linear operation of the transistors and mismatches between the phase lines. These mismatches can be minimized with a careful layout design. Yet, a systematic phase error can be induced between the 0° and 45° phase adders caused by their different operation according to (4) and (5), along with the R_0 and R_{45} resistor mismatches [10]. In [10], it is also proven that the phase error ε_A resulting from the difference in amplitude (A) between the 0° and 45° phase adders outputs is equal to,

$$\varepsilon_A\,(\mathrm{rad}) = \cos^{-1}\left(1 \Big/ \sqrt{1 + (1 + \delta_{\Delta A})^2}\right) - \pi/4 \quad (6)$$

where, $\delta_{\Delta A}$ is the relative amplitude difference ΔA/A.

Furthermore, it is known that controlled phase adders employed in clock and data recovery (CDR) circuits suffer from non-accuracy in phase generation. These phase adders, which usually called phase interpolators create discrete phase steps, however, suffer from inherent non-liner phase control [22]–[25]. This means that a phase error occurs in the output, even in a perfectly balanced circuit fed by perfectly balanced inputs. In our case, an inherent phase error will be produced, even with a phase adder designed perfectly balanced and therefore, compensation techniques must be used to reduce it.

An analysis of the phase error is given in [25] where it is found that, among other factors, it depends on the output load capacitance C_L. In [24] and [25] it is found that the phase interpolation/shifting is based on integration of the output voltage. By focusing on the 45° phase adder an approximation of the inherent phase error ε_{ph} can be calculated. For simplifying the analysis, the drain currents are assumed as pulses, which results to voltages after integration, as shown in Fig.7. If both inputs have the same phase e.g. 0°, the required total current I_{tot} of the phase adder, is calculated from the voltage that swings between 0 and V_{AMP}.

$$I_{tot} = \frac{2C_L V_{AMP}}{T}, \quad (7)$$

where T is the period of the signal. If only a 0° phase is applied at the inputs, the time delay t_{d0} is defined as the time when the voltage is crossing the $\upsilon_{thr} = V_{AMP}/2$ point and it can be calculated as t_{d0} =T/4. In a similar way if both inputs have a 90° phase, the time delay t_{d90} is defined as the time when the voltage is crossing the υ_{thr} point and it can be calculated as $t_{d90} = T/2$. The delay estimation for the 45° combines the integration of two inputs with phase difference of 90° as shown in Fig.7. Between 0 and $T/4$, the output should remain constant at a critical voltage V_{cr}, without charging or discharging the capacitor. Therefore, current $I_{tot}/2$ from the 0° input must be positive, current $I_{tot}/2$ from 90° must be negative and the output voltage $\upsilon(t)$ must remain constant and equal to Vcr for 0 to $T/4$ and begin rising at $T/4$. The voltage output swings between a minimum voltage V_{cr} and a maximum voltage $V_{AMP} - V_{cr}$ with a slope I_{tot}/C_L, as shown in Fig.7, where V_{cr} can be found to be $V_{AMP}/4$. By setting V_{cr} as the initial value for $\upsilon(t)$, then the time t_{d45} from T/4 for the 45° output can be calculated.

$$\begin{aligned}\upsilon(t) &= \frac{I_{tot}}{C_L}\int_{T/4}^{t_{d3}} \mathrm{d}t + V_{cr} \Longrightarrow \frac{V_{AMP}}{2} = \frac{I_{tot}}{C_L}\left(t_{d3} - \frac{T}{4}\right) + V_{cr}\\ &\Longrightarrow t_{d3} = \frac{3\mathrm{T}}{8}\end{aligned} \quad (8)$$

However, in this type of phase adders, the output voltage is not kept constant, between 0 and $T/4$, but it is rising due to the current $I_{tot}/2$ charging the capacitor C_L. Then the voltage V_a which is the voltage at $T/4$ is found to be $3V_{AMP}/8$. Using V_a as the initial value for the output voltage at $T/4$ the delay for the 45° output is given by:

$$\begin{aligned}\upsilon(t) &= \frac{I_{tot}}{C_L}\int_{T/4}^{t'_{d3}} \mathrm{d}t + V_a \Longrightarrow \frac{V_{AMP}}{2}\\ &= \frac{2V_{AMP}}{T}\left(t'_{d3} - \frac{T}{4}\right) + \frac{3V_{AMP}}{8}\\ &\Longrightarrow t'_{d3} = \frac{5T}{16}\end{aligned} \quad (9)$$

The error at the 45° output is then found by comparing with the time delay t_{d3}:

$$\varepsilon_{ph} = -\frac{1}{16}\mathrm{T} \Longrightarrow \varepsilon_{ph}\,(\mathrm{rad}) = -\frac{\pi}{8} \quad (10)$$

This is a systematic error produced considering the current as pulses. Additional errors may affect the final time error, which depends also on $C_L V_{AMP}/I_{tot}$ [25]. The systematic and additional errors are minimized by improving the integration conditions and by making proper design selections. The larger

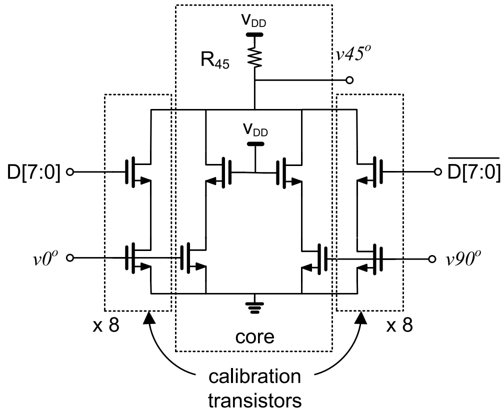

Fig. 8. The 45° phase adder with phase adjustment.

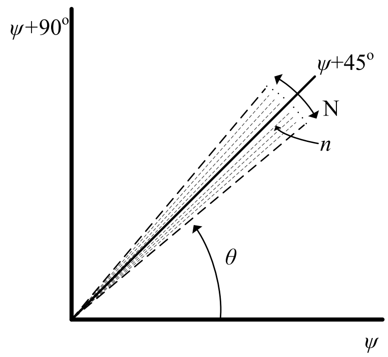

Fig. 9. The phase calibration.

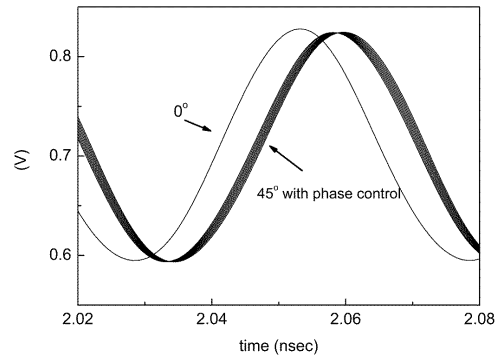

Fig. 10. The output waveform of the phase adder.

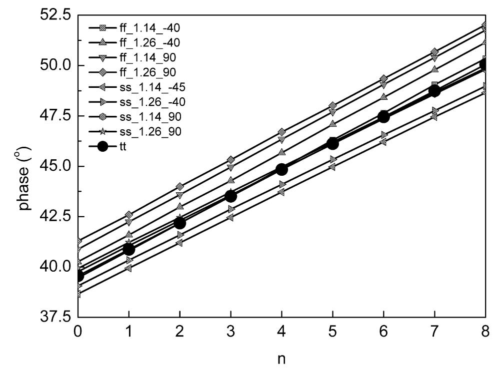

Fig. 11. The phase adjustment vs the control.

the capacitor the better linearity is achieved due to better voltage integration. Therefore, in lower frequencies an extra capacitive load acts beneficially. Operating in tens of gigahertz, the parasitic capacitors are already high enough and therefore no more capacitive load is required. However, a careful design must assure that a large C_L that could reduce the amplitude to a critical level is not presented.

In this paper, controllable phase adders are proposed to compensate for the phase error produced by any of the cases described above, by externally controlling the phases between the 0° and 45° phase adders. Calibration-Transistors (CTs) are placed in both sides of the 45° phase adders, in parallel with the core transistors, as shown in Fig.8.

Totally eight CTs are placed in each side and they are switched on or off in a complementary way using the D[7:0] 8-bit control word. The phase adder is perfectly balanced with four CTs enabled on each side, retaining the balance. In this way we are able to correct negative or positive phase errors by enabling more than four or disabling CTs, respectively. If, for any reason, the adder becomes unbalanced, the preferable number of CTs is activated at the most appropriate side, while the same number of CTs is deactivated at the other side, "moving" the output phase to the corresponding direction. Therefore, the activation/deactivation at each side is taking place in a complementary way with the other side keeping the total number of active CTs always the same; thus, the output current always remains constant, resulting to constant amplitude during the phase correction as well. The output phase shift of the controllable phase adder is calibrated by totally N steps, around the central phase shift of $\psi + 45°$, as shown in Fig.9, where ψ is 0°, 90°, 180°, or 270°. The output phase shift is given by,

$$\theta = (\psi + 45°) + K\frac{2n - N}{2} \cdot 45° + \varepsilon_\theta \tag{11}$$

where, n is the specific step number and $\varepsilon_\theta = \varepsilon_A + \varepsilon_{ph}$ is the total phase error produced by amplitude error and the nonlinear operation of the phase adders; n must take a value suitable to compensate the phase error ε_θ in order for θ to take the desirable value of $\theta = \psi + 45°$. K defines the single-phase step depending on the size ratio between the CTs and the core transistors. K is calculated by,

$$K = \frac{(W/L)_{CT}}{(W/L)_{core} + \frac{N}{2} \cdot (W/L)_{CT}} \tag{12}$$

where, $(W/L)_{CT}$ represents the dimensions of each CT and $(W/L)_{core}$ represents the dimensions of the core transistors. The total number of CTs depends on the number of the steps required. Both the size and the number of CTs must be appropriately selected during the circuit design.

The performance of the phase adder has been examined through simulations using different control words. In Fig.10 the output waveform in time domain is shown, when the calibration is enabled. The achieved phase steps (adjustments) are shown in Fig.11. Eight (8) phase steps are provided, each one of 1.25° phase, leading to a total ±5° phase calibration. It should be noted that n = D[7:0] where only one bit is asserted at any time. This method cannot obviously be applied on the 0° phase adder to correct for e.g. the phase of 90°, as both inputs have the same phase.

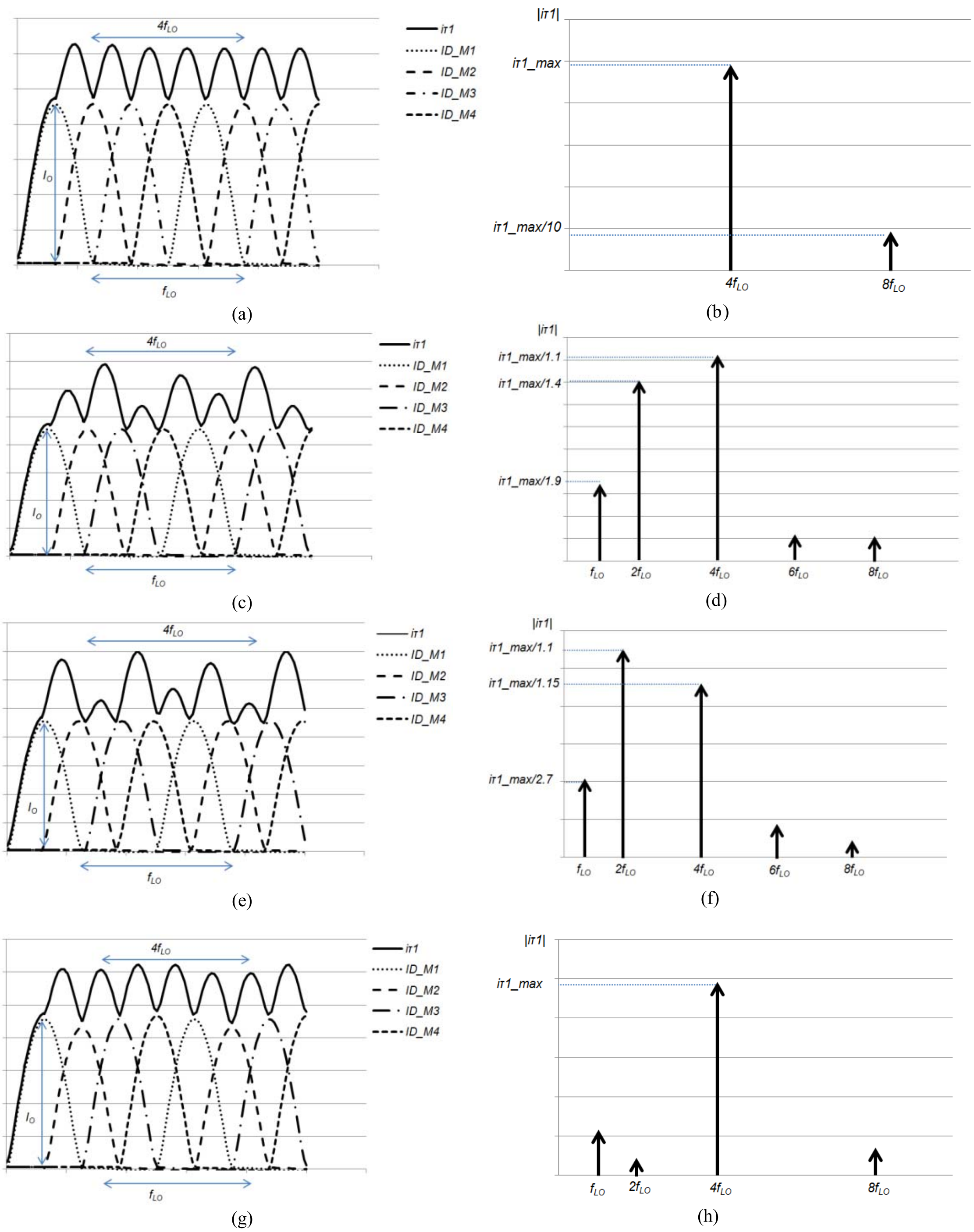

Fig. 12. No phase shift (a, b), ± 5° phase shift (c, d), ± 10° phaseshift (e, f), ± 4% amplitude mismatch (g, h).

C. The 4× SHM Core

The 4× SHM core circuit is shown in Fig.2. It is based on a modified Gilbert cell, where the RF and LO ports have been exchanged and the two bottom transistors have been replaced by two groups of four transistors [11]. The core receives the eight phases from the 20 GHz LO and the RF input at 81 GHz to produce the 1 GHz output. The eight phases have been produced from the LO signal and by means of the phase adders as described in the previous sections.

To get some insight on how the LO frequency is quadrupled, consider the circuit in Figure 2. The phase adders generate the $V(0°)$, $V(90°)$, $V(180°)$, $V(270°)$ signals. These signals are then converted to the rectified (by biasing) drain currents I_{D_M1} to I_{D_M4}, of the transistors $M1$-M4, with equal amplitudes and 90° difference among one another. By using the Linear Superposition (LS) technique the higher frequency $(4f_{LO})$ output current i_{T1} is produced.

$$i_{T1} = \frac{4}{\pi}\mathrm{I}_0\left(1 - \frac{2}{15}cos(4\omega_0 t) - \cdots\right) \tag{13}$$

where I_0 is the amplitude of the current $I_{D_M x}$ (x ranges for 1 to 4). The superposition cancels the fundamental, second and

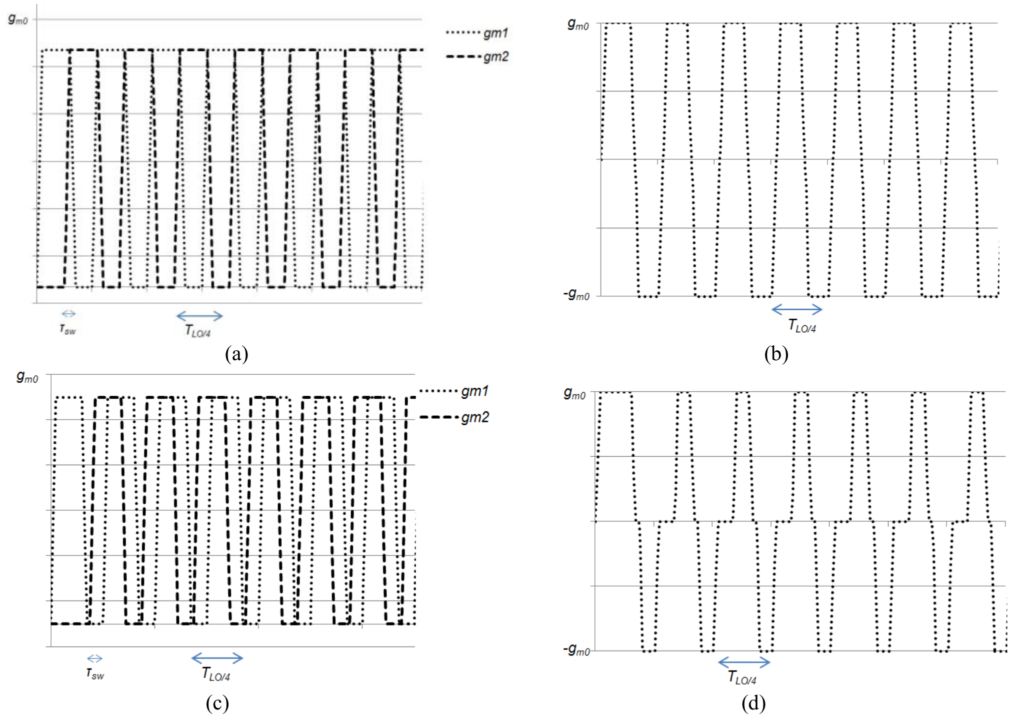

Fig. 13. Waveforms occurring in the switched transconductor SHM for the case with equal ON- and OFF-switching times τ_{sw}.

third order harmonics and leaves the fourth order term [26]. This method is more readily comprehended graphically for i_{T1} in Fig.12(a). The rms current values at each frequency are given in Fig.12(b). Obviously, the switching stage of a SHM performs both functions of switching and $4f_{LO}$ frequency generation. The same operation occurs for the other four LO transistors (45°, 135°, 225°, 315°) and the resulting current, i_{T2}, is 180° out of phase with i_{T1}. If the input phase varies by ±5° for a frequency of 20 GHz the current amplitude of the 4$^{\text{th}}$ harmonic decreases slowly. However, a significant increase in the amplitude of the fundamental and 2$^{\text{nd}}$ harmonic is observed as shown in Fig.12(c) and Fig.12(d). As we deviate beyond ±10°, the output amplitude of the 2$^{\text{nd}}$ harmonic begins to dominate and the x4 operation breaks down as depicted in Fig.12(e) and Fig.12(f). Simulation results presented in Figures 12(a)-(f) show that the suppression of fundamental and 2$^{\text{nd}}$ harmonics is relatively sensitive to the phase mismatch (assuming perfect amplitude match from all phase shifted signals) and decreases rapidly as the phase mismatch increases. It is also shown that the amplitude of currents i_{T1} and i_{T2} is also affected by the mismatches. Harmonic suppressions versus amplitude mismatches are also simulated as shown in Fig.12(g) and Fig.12(h). For the amplitude mismatch up to 4%, it is clear that the harmonic suppression variations are insignificant.

Furthermore, for the switched transconductor SHM shown in Fig.2 $v_{out}(t) = -g_{meff}(t)\cdot \mathrm{R}\cdot \mathrm{v}_{RF}(t)$ where $g_{meff}(t) = g_{m1}(t) - g_{m2}(t)$.

Supposing that the transconductance time function for $g_{m1}(t)$ and $g_{m2}(t)$ is a trapezoid function, shown in Fig.13(a) and Fig.13(b), with equal on- and off-switching times τ_{sw}, a first-order approximation of the conversion gain CG of the mixer becomes as in [27]:

$$CG = \frac{2}{\pi}\left(\frac{sin(\pi \cdot 4f_{LO} \cdot \tau_{SW})}{\pi \cdot 4f_{LO} \cdot \tau_{SW}}\right) \cdot g_{m0} \cdot R_L \tag{14}$$

where $g_{m0} = \max(g_{m1}(t)) = \max(g_{m2}(t))$. For low LO frequencies, or for $\tau_{sw} = 0$, the CG is equal to the familiar $2/\pi$ times $g_{m0}R_L$, corresponding to mixing with a square wave. If the phase difference between g_{m1} and g_{m2} deviates from 180°, then g_{meff} can be approximated by a triangular waveform as shown in Fig.13(c) and Fig.13(d). In that case the fundamental Fourier coefficient is $8/\pi^2$ instead of $4/\pi$ with an additional factor ½ from the multiplication. Thus:

$$CG = \frac{4}{\pi^2} \cdot g_{m0} \cdot R_L \tag{15}$$

Conversion gain is optimum for equal on- and off-switching times and when $g_{m1}(t)$ and $g_{m2}(t)$ waveforms remain also equal and are time shifted by $1/(2\cdot 4\cdot f_{LO})$. Obviously, as the g_{eff} waveform deviates for the rectangular or trapezoid shape the conversion gain goes down. In that sense, the proposed method improves the performance of the mixer by providing nearly perfect 45° out-of-phase LO signals. Consequently, nearly perfect 180° out-of-phase currents i_{T1} and i_{T2} switching at $4f_{LO}$ are generated, going into the transconductance stage, and thus double-balanced subharmonic mixing occurs providing optimum gain and high-levels of isolation between the ports.

The output of the 4× LO generation circuit (mixing transistors) is also not sensitive to relatively small amplitude variations. However, by using Calibration-Transistors (CTs) an

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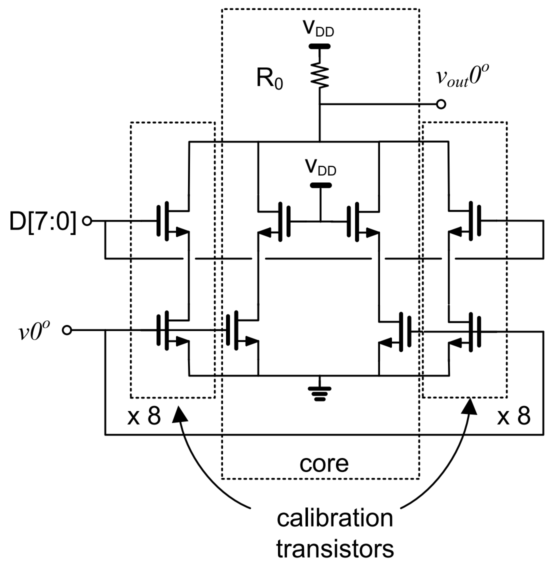


Fig. 14. The proposed schematic of the 0° phase adder with gain adjustment.

extra feature that is offered is the gain calibration in case the amplitudes of 0° and 45° phase shifted signals do not match, even after selecting the appropriate values for R_0 and R_{45}. The corresponding CTs are now enabled/disabled the same way (not complementary) on both sides. The proposed schematic of a 0° phase adder with gain adjustment is shown in Fig.14.

The circuitry that could be utilized to detect the mismatches consists of an envelope detector, a LPF and an amplifier followed by and ADC. The amplitude of the IF signal is detected, amplified, filtered and passed on to the baseband DSP that determines the value of the D[7:0] 8-bit control word.

Finally, the purpose of the inductors in the mixer core is to increase the LO voltage swing at the source terminal of the RF transistors, providing higher conversion gain for the mixer at lower LO powers than would be required without the enhancement inductors.

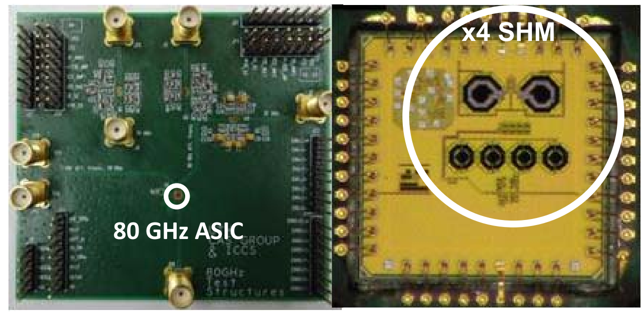
III. Implementation and Experimental Results

The down-conversion subharmonic mixer presented so far is designed and fabricated on the TSMC 65-nm 1P9M CMOS MS/RF low power (LP) process optimized for lower leakage currents. The die area is 0.85×0.8 mm^2 excluding the pads.

The bare dies have been attached directly on a chip-on-board (CoB), 82.5 × 76 mm printed circuit board (PCB), with 4 layers stackup and ENEPIG (electroless nickel, electroless palladium, immersion gold) finished pads.

ASTRA® MT Very Low-loss Laminate Material has been used, offering a Dielectric constant (Dk) of 3.00±0.05 and a Dissipation factor (Df) of 0.0017±0.0005. The dielectric thickness is 0.127 mm and the copper thickness is 9um. All dies are recessed into the PCB, to achieve a co-planar layout minimizing wire bond inductance and have been attached directly to the ground plane with conductive epoxy. 50um Au Ribbon bonds and 25um Au wire bonds have been used.

The photograph on the left side of Fig.15 shows the realized chip-on-board PCB including the 80 GHz ASIC and



(a) (b)

Fig. 15. Photograph showing the realized chip-on-board PCB (a) and, photograph showing the 80GHz ASIC including the x4 SHM (b).

the x6 active broadband frequency multiplier chips, whereas the microphotograph of the 80 GHz ASIC incorporating the x4 SHM is shown on the right. A standalone x6 active multiplier is also included for performance characterization.

The test setup is given in Fig.16. The 81 GHz RF signal is generated by a synthesized signal generator (Analog Devices HMC-T2240, 10MHz – 40 GHz) followed by a Balanced to Unbalanced Transformer (Marki Microwave BAL-0520, 5–20 GHz) and two x6 active broadband frequency multiplier chips utilizing GaAs pHEMT technology (Analog Devices HMC1110). A 1 GHz - 20 GHz Synthesized CW Generator (Keysight Technologies 83711B) is used as the 20 GHz LO source. The output IF signal is measured using a Balanced to Unbalanced Transformer (Marki Microwave BAL-0003, 200 KHz–3 GHz) connected to the spectrum analyzer (Keysight Technologies E4440A PSA Spectrum Analyzer, 3 Hz to 26.5 GHz). The DC supply voltage was set to 1.2 V, the RF input signal was −20 dBm @ 13.5 GHz, and the LO signal was 12 dBm @ 20 GHz. Therefore, the desired output signal was seen at 1 GHz ($6f_{RF} - 4f_{LO}$).

A typical output spectrum is shown in Fig.17. The proposed method has the benefit of reducing the spurious interferers possible at the IF port as it improves the accuracy of the octet-phase generator circuit, which in turn provides nearly perfect 45° out-of-phase LO signals to the mixing transistors.

Figure 18 shows the measured conversion gain (CG) of the mixer with the corresponding LO power. With a fixed RF power at 81 GHz (i.e. 13.5 × 6 GHz) while sweeping the LO power, the CG of the mixer can be calculated as:

$$CG(dB) = P_{IF} - (P_{RF} - IL_{RF\_BAL} + CG_{MULT}) + IL_{IF\_BAL} \tag{16}$$

where P_{IF} is the output power obtained from the spectrum analyzer, P_{RF} is the input RF power applied from the signal generator, CG_{MULT} is the conversion gain of the frequency multiplier, $IL_{RF_BAL} = 4.5$dB is the insertion loss of the RF balun and $IL_{IF_BAL} = 6$dB is the insertion loss of the IF balun. The optimum CG is ~ -8 dB at the LO power of 12 dBm and is achieved by calibrating the phase adder's output signal phase. A step number of $n = 5$ (46.25° out of phase instead of 45°) ensures the optimum performance. Optimum simulated CG is −7dB for $n = 4$. A spectrum analyzer with frequency coverage up to 61 GHz

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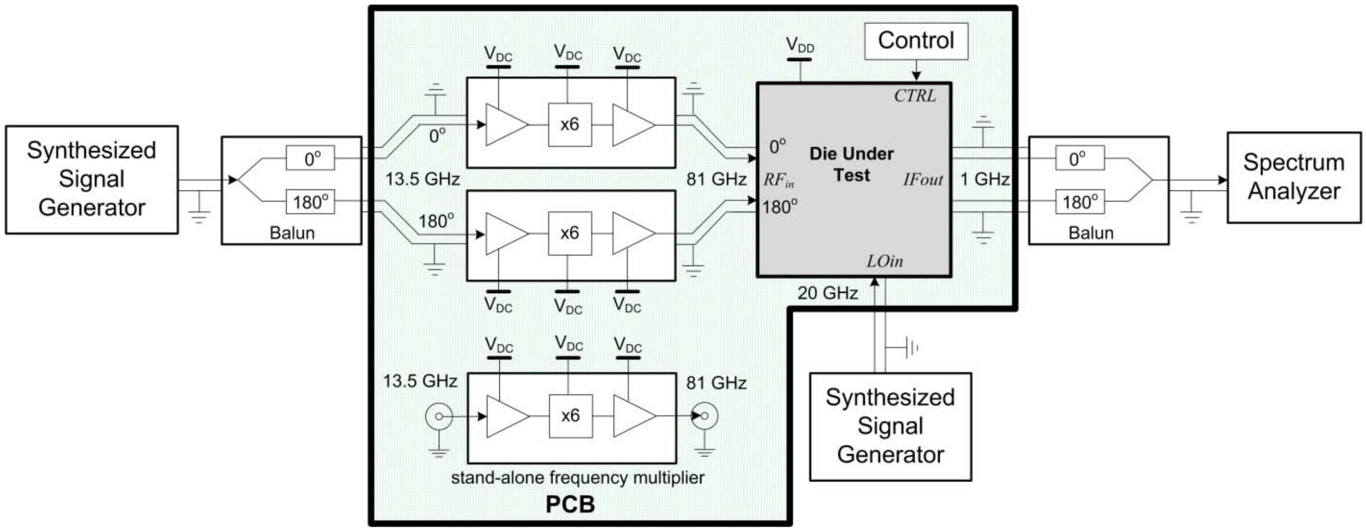

Fig. 16. Block diagram of the 80 GHz 4× sub-harmonic mixer test setup.

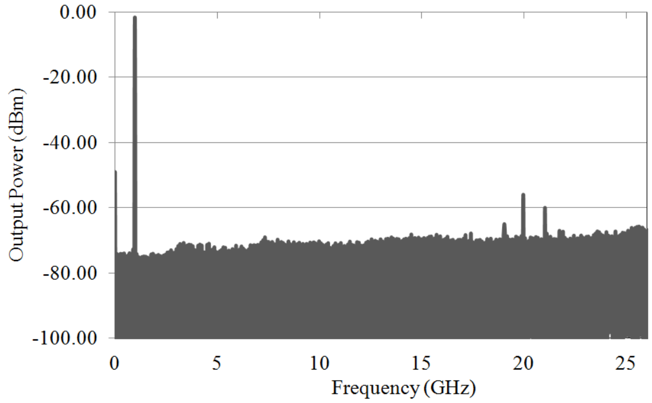

Fig. 17. Measured mixer output spectrum with -20 dBm RF power and 12 dBm LO power.

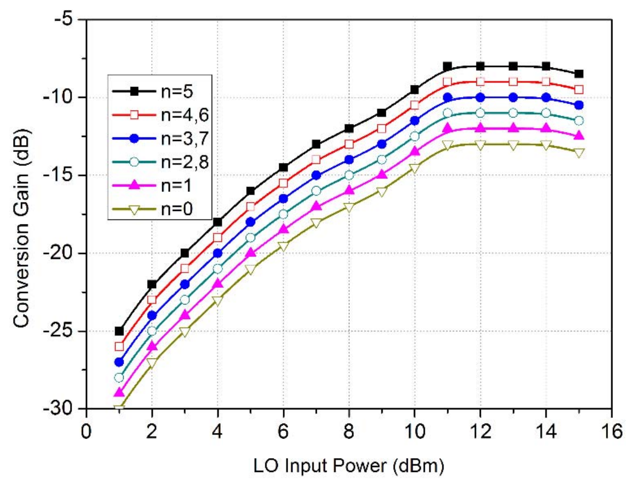

Fig. 18. Measured CG versus LO input power. The step number n is swept from 0 to 8 in steps of 1.

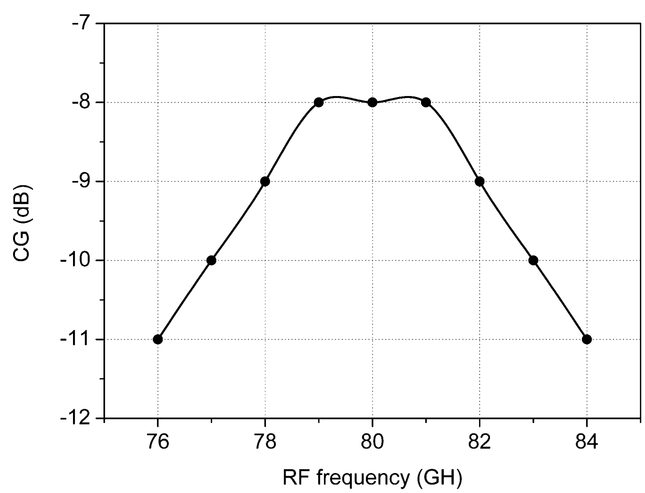

Fig. 19. Measured conversion gain of the 80 GHz sub-harmonic balanced mixer for $f_{IF} = 1$ GHz.

would be needed to better show the harmonic suppression versus the phase mismatches. Figure 19 shows the conversion gain of the mixer when IF is fixed at 1 GHz. The mixer is broadband with a conversion gain of -8 to -11 dB from 76–84 GHz.

After the mixer stage, a source-follower buffer stage is used to provide the impedance matching to the 50Ω. Therefore, there was no gain in this stage that would contribute to the conversion gain of the mixer. For the RF_{in} input port, distributed microstrip matching have been performed using open/short stubs on the PCB layer stack-up. PCB matching on the ASTRA® MT Very Low-loss Laminate Material has lower loss with the respect to the IC matching that is based on resistive type dielectrics. This is mandatory for mmwave applications. The S-parameters file of the internal circuitry has been exported and then 3D EM analysis of the ribbon bonding in between the PCB trace and the MMIC pads has been performed in order to move the S-parameters reference plane from the MMIC internal structure out to the PCB pad level. A full system level simulation of the PCB to MMIC transition also took place in order to verify the RF matching performance over the frequency band of interest. For the LO_{in} input port, a reasonably good input impedance match to 50 Ω is achieved since the input to the active balun is approximately that of the common-gate circuit, $Z_{in} = 1/g_m$, considering that the resistor R_b is large.

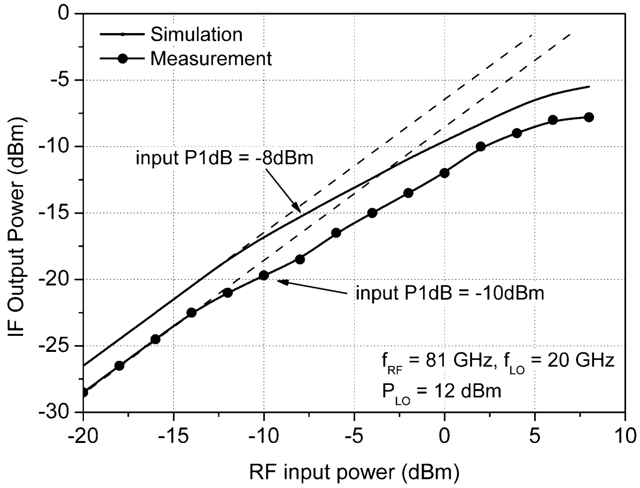

Fig. 20. Measured 1dB compression point (P1dB).

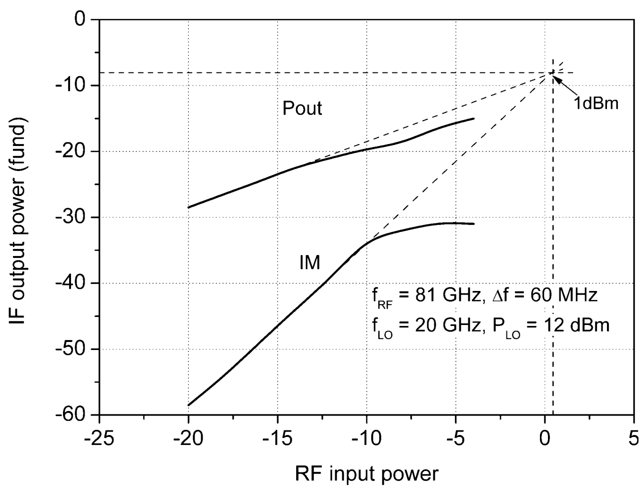

Fig. 21. Measured input third-order intercept point (IIP3).

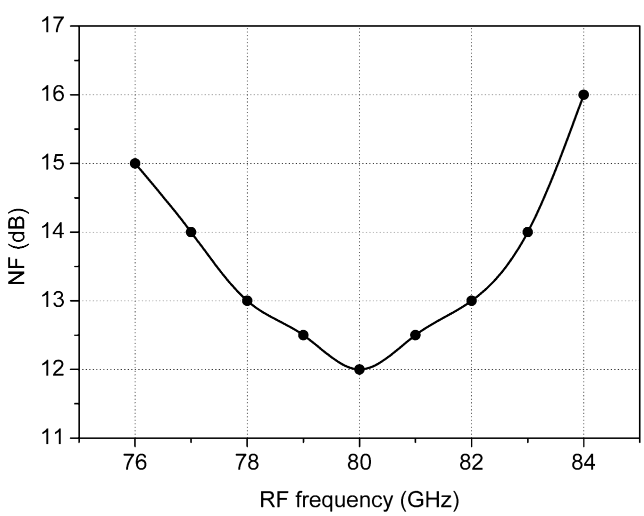

Fig. 22. Measured NF versus RF input frequency (multiplier/SHM combination).

The 1-dB compression (P1dB) and input third-order intercept (IIP3) points of the proposed mixer shown in Fig.20 and Fig.21 respectively, are extracted from the measurement data under the following assumptions which are clearly valid in our case: (i) the SHM dominates both the overall P1dB and IIP3 points of the cascaded system (i.e. balun-multiplier-SHM-balun) due to the high P1dB and IIP3 of the preceding and the succeeding stages and (ii), the insertion losses and the gain of the preceding (balun and multiplier) and the succeeding stages (balun) are known. The linearity performance is measured via a two-tone test at 81GHz (i.e. 13.5 × 6 GHz) and 81.060 GHz (i.e. 13.51 × 6 GHz), along with an LO input set at 12 dBm. The simulated P1dB is −8 dBm and IIP3 is 2 dBm. The measured Conversion Gain, P1dB, and IIP3 are all slightly lower than the simulated values, and this is probably due to the lower LO signal at the switching stage. All devices in the 4× subharmonic mixer core are biased near their threshold voltage and thus, the performance of the mixer greatly depends on the signal from the LO. Simulations are showing that the IIP2 of the SHM mixer itself is greater than 33 dBm.

TABLE I

MEASURED LO-IF ISOLATION WITH PHASE CORRECTION

Phase correction	LO-IF isolation (dB)
n = 0	-55
n = 1	-58
n = 2,8	-60
n = 3,7	-63
n = 4,6	-67
n = 5	-72

TABLE II

GAIN OF THE SHM OVER VOLTAGE & TEMPERATURE VARIATIONS FOR DIFFERENT V_{BS}

Supply voltage (VDD)	Bulk Voltage of NMOS / PMOS $V_{BSn} = V_{BSp}$=0V		
	@ -40 ºC	@ 27 ºC	@ 95 ºC
1.2V	-8	-8	-9.5
1.1V	-8	-8	-10
1.0V	-9	-9.5	-10.5
Supply voltage (VDD)	Bulk Voltage of NMOS / PMOS V_{BSn} = 0.08V &V_{BSp}=1.12V		
	@ -40 ºC	@ 27 ºC	@ 95 ºC
1.2V	-8	-8	-9
1.1V	-8	-8	-9.5
1.0V	-8	-9	-10
Supply voltage (VDD)	Bulk Voltage of NMOS / PMOS V_{BSn} = 0.1V &V_{BSp}=1.1V		
	@ -40 ºC	@ 27 ºC	@ 95 ºC
1.2V	-8	-8	-8
1.1V	-8	-8	-9
1.0V	-8	-8	-9.5
Supply voltage (VDD)	Bulk Voltage of NMOS / PMOS V_{BSn} = 0.15V &V_{BSp}= 1.05V		
	@ -40 ºC	@ 27 ºC	@ 95 ºC
1.2V	-8	-8	-8
1.1V	-8	-8	-8
1.0V	-8	-8	-9
Supply voltage (VDD)	Bulk Voltage of NMOS / PMOS V_{BSn} = 0.23V &V_{BSp}= 0.97V		
	@ -40 ºC	@ 27 ºC	@ 95 ºC
1.2V	-8	-8	-8
1.1V	-8	-8	-8
1.0V	-8	-8	-8

The noise figure of the frequency multiplier/SHM combination is degraded due to the loss of the input and the output baluns. It is well known that when a component with L (dB) loss is placed at the input of a system, the noise figure will be

TABLE III

NF OF THE FREQUENCY MULTIPLIER/SHM COMBINATION OVER VOLTAGE & TEMPERATURE VARIATIONS FOR DIFFERENT V_{BS}

Supply voltage (VDD)	Bulk Voltage of NMOS / PMOS V_{BSn} = V_{BSp}=0V		
	@ -40 ºC	@ 27 ºC	@ 95 ºC
1.2V	12	12	13
1.1V	12	12	14
1.0V	12.5	13	15
Supply voltage (VDD)	Bulk Voltage of NMOS / PMOS V_{BSn} = 0.08V &V_{BSp}=1.12V		
	@ -40 ºC	@ 27 ºC	@ 95 ºC
1.2V	12	12	12.5
1.1V	12	12	14
1.0V	12	12.5	15
Supply voltage (VDD)	Bulk Voltage of NMOS / PMOS V_{BSn} = 0.1V &V_{BSp}=1.1V		
	@ -40 ºC	@ 27 ºC	@ 95 ºC
1.2V	12	12	12
1.1V	12	12	13
1.0V	12	12	14.5
Supply voltage (VDD)	Bulk Voltage of NMOS / PMOS V_{BSn} = 0.15V &V_{BSp}= 1.05V		
	@ -40 ºC	@ 27 ºC	@ 95 ºC
1.2V	12	12	12
1.1V	12	12	12
1.0V	12	12	13
Supply voltage (VDD)	Bulk Voltage of NMOS / PMOS V_{BSn} = 0.23V &V_{BSp}= 0.97V		
	@ -40 ºC	@ 27 ºC	@ 95 ºC
1.2V	12	12	12
1.1V	12	12	12
1.0V	12	12	12

TABLE IV

IIP3 OF THE SHM OVER VOLTAGE & TEMPERATURE VARIATIONS FOR DIFFERENT V_{BS}

Supply voltage (VDD)	Bulk Voltage of NMOS / PMOS V_{BSn} = V_{BSp}=0V		
	@ -40 ºC	@ 27 ºC	@ 95 ºC
1.2V	1	1	-1
1.1V	1	1	-2
1.0V	0	-1	-3
Supply voltage (VDD)	Bulk Voltage of NMOS / PMOS V_{BSn} = 0.06V &V_{BSp}=1.14V		
	@ -40 ºC	@ 27 ºC	@ 95 ºC
1.2V	1	1	-0.5
1.1V	1	1	-1.5
1.0V	1	-0.5	-2
Supply voltage (VDD)	Bulk Voltage of NMOS / PMOS V_{BSn} = 0.08V &V_{BSp}=1.12V		
	@ -40 ºC	@ 27 ºC	@ 95 ºC
1.2V	1	1	1
1.1V	1	1	-0.5
1.0V	1	1	-1
Supply voltage (VDD)	Bulk Voltage of NMOS / PMOS V_{BSn} = 0.13V &V_{BSp}= 1.07V		
	@ -40 ºC	@ 27 ºC	@ 95 ºC
1.2V	1	1	1
1.1V	1	1	1
1.0V	1	1	-0.5
Supply voltage (VDD)	Bulk Voltage of NMOS / PMOS V_{BSn} = 0.2 &V_{BSp}= 1.0V		
	@ -40 ºC	@ 27 ºC	@ 95 ºC
1.2V	1	1	1
1.1V	1	1	1
1.0V	1	1	1

$NF = NF_0 + L$ where NF_0 is the noise figure in the absence of the lossy component. Furthermore, using the Friis's formula it is easily found that the NF_0 of the system under test is degraded further due to the output balun used.

The loss L of the BAL-0520 is 4.5dB and the loss L of the BAL-003 is 6dB typically thus, the noise figure of the frequency multiplier followed by the subharmonic mixer can be then calculated. The NF of the amplified frequency multiplier (HMC1110) is not reported thus, the measured NF of the SHM cannot be estimated.

The minimum measured NF of the frequency multiplier/ SHM combination is $\sim$12 dB, as shown in Fig.22 whereas the simulated noise figure of the mixer is 15 dB. Noise figure measurements have been made using the 8970SNoise Figure Measurement System (10 MHz to 26.5 GHz). The IF is kept at the fixed value of 1-GHz during this measurement. Simulation and measurement results show that typical phase/amplitude mismatches between the octet-phase LO signals do not significantly affect noise figure. This is due to the fact that the biggest contributor for the noise figure of the mixer is the flicker noise of the transconductance (RF) stage devices. The switched transconductor mixer introduces significantly more $1/f$ noise due to the transconductance devices compared to a conventional active mixer. In contrast, the switched transconductor has negligible $1/f$ and thermal noise due to the switch devices. In the switched transconductor, the noise goes down together with the useful signal, while in the conventional mixer the signal drops, and noise increases due to the contribution of the switching [27].

Very high isolation between the ports, crucial for direct conversion receivers, was measured. The simulated 2LO–RF and the 4LO–RF suppression values are very high (59 dB and 64 dB respectively), while the measured LO-IF isolation is 72 dB, the measured LO-RF is 75 dB and the simulated 2LO–IF and the 4LO–IF suppression values are 58 dB and 62 dB respectively. Table I reports measurement results for the LO-IF isolation showing the efficiency of the proposed technique.

To access the body terminals of the polyphase filter's MOS devices, triple-well transistors and a pair of body bias signals were used: one signal biases the NMOS transistors and the other one biases the PMOS. Tables II, III and IV, show the effect of body bias on the different supply voltage and temperature cases, targeting optimum performance in terms of maximum conversion gain, maximum IIP3 and minimum noise figure.

For instance, for supply voltage equal to 1.0 V and $T = 95°C$, maximum conversion gain and minimum noise figure are reached when $V_{BSn} = 0.23V$ and $V_{BSp} = 0.97V$. For the same case, maximum IIP3 occurs when $V_{BSn} = 0.2$ and $V_{BSp} = 1.0V$.

The DC power consumption for the mixer core was approximately 7 mW. For the entire design including the RF balun (11 mW), the polyphase filter (50 mW), the phase adder w/phase adjustment (145 mW) and the mixer core as well, the power consumption was measured to be 213 mW.

Table V compares the implemented architecture to state-of-the-art CMOS implementations that have already been

TABLE V
PERFORMANCE SUMMARY AND COMPARISON

PARAMETERS	[11] JSSC'08	[28] JSSC'05	[12] MWCL'15	[29] MWCL'16	[30] MWCL'08	[31] RFIT'16	THIS WORK
VDD (V)	2.75	5	1.5	1.2	-	0.8	1.2
DC Power (mW)	113	62	17 (core only)	74	58	1	213 (7mw core)
f_{RF} (GHZ)	12	77	93	170	70	60	80
CG (dB)	6	0.7	3.5	+8[1]	-1.5	5.9	-8[2]
LO harm.	4	2	4	2	2	2	4
P_{LO} (dBm)	10	10	10	4	10	-3.5	12
P_{1dB} (dB)	-12	-8	-9.2	N/A	-11.9	-19.5	-10
IIP3 (dBm)	-2	+6	N/A	N/A	N/A	-9.5	1
NF (dB)	18	23	15.5	26	N/A	N/A	15
LO-RF isolation (dB)	71	>30	55	N/A	>47	>49	72
Technology	CMOS 180nm	SiGe	CMOS 65-nm	32-nm SOI	CMOS 90-nm	CMOS 90-nm	CMOS 65-nmLP
Chip size (mm^2)	850x850	900x860	780x480	0.75	0.32	0.03	850x800
Features	w/ IF buffer (no gain)	balanced w/ IF amp[3]	balanced w/ IF amp	balanced w/ IF amp	Gilbert-cell w/ IF buffer (no gain)	Single-ended w/ IF amp	w/ IF buffer (no gain)

[1] simulated conversion gain of the mixer only is -23dBm
[2]no amplification stage follows the mixer core
[3] CG=-10.3 w/o IF amp

reported in literature. The measurements obtained herein are very promising despite the use of the LP process, and the absence of amplification after the mixer core; as noted earlier, limited gain ability was expected due to the LP process implementation. The proposed architecture has not been optimized for low power operation. Moreover, circuits fabricated in 65-nm LP technology are expected to require a higher supply voltage and to dissipate more power than their 90nm GP versions operating in the same frequency range [32]. Nevertheless, efficient post-silicon tuning over voltage and temperature variations along with the 5.5 dB CG improvement using the phase calibration mechanism are of greater importance driving the main aspects of the present work.

IV. CONCLUSION

In this paper the design, implementation and testing of a novel mm-wave 76-84 GHz 4× subharmonic mixer topology in 65-nm LP CMOS is reported. A conversion gain of approximately −8 dB, an input-referred 1-dB compression point of −10 dBm, and a single sideband noise figure of 15dB was obtained. The proposed mixer also presents a good isolation between the LO and the RF ports. The design of this mixer is robust against voltage and temperature variations. A comparison with state of the art mixers is also given. The results of the present work demonstrate for the first time an integrated mixer topology, incorporating a balun, a polyphaser filter and a phase adder with error correction, with excellent performance at these high frequencies, suitable for mm-wave wireless applications even using the slower CMOS LP node. This technique is useful in other applications, beyond SHMs, where phase mismatch compensation is required.

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REFERENCES

[1] R. Svitek and S. Raman, "DC offsets in direct-conversion receivers: Characterization and implications," *IEEE Microw. Mag.*, vol. 6, no. 3, pp. 76–86, Sep. 2005.
[2] K. Kivekas, A. Parssinen, and K. A. I. Halonen, "Characterization of IIP2 and DC-offsets in transconductance mixers," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 48, no. 11, pp. 1028–1038, Nov. 2001.
[3] R. G. Meyer, W. D. Mack, and J. J. E. M. Hageraats, "A 2.5-GHz BiCMOS transceiver for wireless LAN's," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2097–2104, Dec. 1997.
[4] K. Nimmagadda and G. M. Rebeiz, "A 1.9 GHz double-balanced subharmonic mixer for direct conversion receivers," in *Proc. IEEE RFIC Symp.*, Phoenix, AZ, USA, May 2001, pp. 253–256.
[5] Z. Zhang, L. Tsui, Z. Chen, and J. Lau, "A CMOS self-mixing-free front-end for direct conversion applications," in *Proc. IEEE ISCAS*, May 2001, pp. 386–389.
[6] S. A. S. Mohamed and Y. Manoli, "Design of low-power direct-conversion RF front-end with a double balanced current-driven subharmonic mixer in 0.13 μm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 5, pp. 1322–1330, May 2013.
[7] P. Upadhyaya, M. Rajashekharaiah, D. Heo, and Y.-J. E. Chen, "A high IIP2 doubly balanced sub-harmonic mixer in 0.25-μm CMOS for 5-GHz ISM band direct conversion receiver," in *Proc. IEEE RFIC Symp.*, Jun. 2005, pp. 175–178.
[8] B. R. Jackson and C. E. Saavedra, "A CMOS subharmonic mixer with input and output active baluns," *Microw. Opt. Technol. Lett.*, vol. 48, no. 12, pp. 2472–2478, Dec. 2006.
[9] R. M. Kodkani and L. E. Larson, "An integrated 50-GHz SiGe subharmonic mixer/downconverter with a quadrature ring VCO," in *Proc. Topical Meeting Silicon Monolithic Integr. Circuits RF Syst.*, Jan. 2007, pp. 223–226.
[10] K.-J. Koh, M.-Y. Park, C.-S. Kim, and H.-K. Yu, "Subharmonically pumped CMOS frequency conversion (up and down) circuits for 2-GHz WCDMA direct-conversion transceiver," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 871–884, Jun. 2004.
[11] B. R. Jackson and C. E. Saavedra, "A CMOS ku-band 4× subharmonic mixer," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1351–1359, Jun. 2008.
[12] T. N. Huang *et al.*, "A CMOS W-band 4× quasi-subharmonic mixer," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 6, pp. 385–387, Jun. 2015.
[13] M. W. Chapman and S. Raman, "A 60-GHz uniplanar MMIC 4× subharmonic mixer," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 11, pp. 2580–2588, Nov. 2002.
[14] T. Yamaji, H. Tanimoto, and H. Kokatsu, "An I/Q active balanced harmonic mixer with IM2 cancelers and a 45° phase shifter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 1998, pp. 368–369.

[15] J. Kaukovuori, K. Stadius, J. Ryynanen, and K. A. I. Halonen, "Analysis and design of passive polyphase filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 10, pp. 3023–3037, Nov. 2008, doi: 10.1109/TCSI.2008.917990.

[16] M. Kaltiokallio, J. Ryynänen, and S. Lindfors, "Active polyphase filter analysis," in *Proc. IEEE Int. Symp. Circuits Syst.*, Paris, France, May/Jun. 2010, pp. 1125–1128.

[17] G. Souliotis, F. Plessas, F. Liakou, and M. Birbas, "A 90 nm CMOS 15/60 GHz frequency quadrupler," *Int. J. Electron.*, vol. 100, no. 11, pp. 1529–1545, 2013.

[18] F. Tillman and H. Sjoland, "A polyphase filter based on CMOS inverters," *Analog Integr. Circuits Signal Process.*, vol. 50, no. 1, pp. 7–12, Jan. 2007.

[19] E. M. Cherry and D. E. Hooper, "The design of wide-band transistor feedback amplifiers," *Proc. Inst. Elect. Eng.*, vol. 110, no. 2, pp. 375–389, Feb. 1963.

[20] H. Rashtian, A. H. M. Shirazi, and S. Mirabbasi, "On the use of body biasing to improve linearity in low LO-power CMOS active mixers," *Microelectron. J.*, vol. 45, no. 8, pp. 1026–1032, 2014.

[21] M.-T. Hsu, K.-L. Wu, and W.-C. Chiu, "Systematic approaches of UWB low-power CMOS LNA with body biased technique," *Wireless Eng. Technol.*, vol. 6, no. 3, pp. 61–77, 2015.

[22] S. Sidiropoulos and M. A. Horowitz, "A semidigital dual delay-locked loop," *IEEE J. Solid-State Circuits*, vol. 32, no. 11, pp. 1683–1692, Nov. 1997.

[23] P. K. Hanumolu, G.-Y. Wei, and U. K. Moon, "A wide-tracking range clock and data recovery circuit," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 425–429, Feb. 2008.

[24] G. Souliotis, C. Laoudias, F. Plessas, and N. Terzopoulos, "Phase interpolator with improved linearity," *Circuits, Syst. Signal Process.*, vol. 35, no. 2, pp. 367–383, Feb. 2016.

[25] A. Tsimpos, A. C. Demartinos, G. Souliotis, and S. Vlassis, "Multi-rate phase interpolator for high speed serial interfaces," *Microelectron. J.*, vol. 54, pp. 40–47, Aug. 2016.

[26] D. Huang *et al.*, "Terahertz CMOS frequency generator using linear superposition technique," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2730–2738, Dec. 2008.

[27] E. A. M. Klumperink, S. M. Louwsma, G. J. M. Wienk, and B. Nauta, "A CMOS switched transconductor mixer," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1231–1240, Aug. 2004.

[28] J. Hung, T. M. Hancock, and G. M. Rebeiz, "A 77 GHz SiGe subharmonic balanced mixer," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2167–2173, Nov. 2005.

[29] D. Parveg *et al.*, "CMOS I/Q subharmonic mixer for millimeter-wave atmospheric remote sensing," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 4, pp. 285–287, Apr. 2016.

[30] J.-H. Tsai, H.-Y. Yang, T.-W. Huang, and H. Wang, "A 30–100 GHz wideband sub-harmonic active mixer in 90 nm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 8, pp. 554–556, Aug. 2008.

[31] C.-H. Chi and H.-R. Chuang, "A 60-GHz CMOS ultra-low-power single-ended sub-harmonic mixer in 90-nm CMOS," in *Proc. IEEE Int. Symp. Radio-Freq. Integr. Technol. (RFIT)*, Taipei, Taiwan, Aug. 2016, pp. 1–3.

[32] S. P. Voinigescu *et al.*, "CMOS SOCs at 100 GHz: System architectures, device characterization, and IC design examples," in *Proc. IEEE Int. Symp. Circuits Syst.*, New Orleans, LA, USA, May 2007, pp. 1971–1974.

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