Journal of Circuits, Systems, and Computers
Vol. 16, No. 4 (2007) 577–588

World Scientific
www.worldscientific.com

THEORETICAL AND EXPERIMENTAL EVALUATION OF THE PHASE NOISE BEHAVIOR OF A DUAL-LOOP FREQUENCY SYNTHESIZER FOR 5-GHz WLANs

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Revised 8 May 2007

This paper presents the analysis and experimental evaluation of a modified dual-loop phase-locked loop synthesizer, using the phase noise transfer functions resulting from the linear model of the synthesizer. The different arrangement in the high-frequency loop, in contrast to previous reported series-connected dual-loop topologies, offers various advantages, such as improved phase noise, finer resolution, and lower spurious levels. Discrete elements are used to implement a prototype system for testing. This adds to the flexibility of the design and allows for experimental optimization of the loop trade-offs. The synthesizer generates signals in the 4850 MHz to 5050 MHz range with a 10 MHz resolution and can match the specifications for wireless LANs operating at 5 GHz. The design resulted in a prototype with very good characteristics suitable for future integration.

Keywords: Phase-locked loop; frequency synthesizer; dual-loop architecture; wireless receiver; phase noise.

1. Introduction

Due to the demands for modern WLAN technology in recent years, there is increasing need for systems operating at high radio frequencies in the range of 5 GHz. A critical subsystem for these applications is the frequency synthesizer which must exhibit low phase noise over a wide bandwidth, fast settling time and low spur level.

The demand for wide bandwidth and low phase noise leads us to give increased attention to the system design. In this work, we reconsider dual-loop designs and put them in the context of broadband design at the 5 GHz range. We propose a modified architecture, which through analysis and measurements proved to exhibit superior phase noise performance compared to other reported architectures. To demonstrate the validity of our approach the synthesizer is implemented using discrete components. Measurements give comparable results to theory and show that the proposed modified dual-loop architecture can lead to superior performance.

Integer N, fractional N, and $\Delta\Sigma$ fractional N synthesizers are very popular architectures. Each one offers different advantages, but also suffers from various disadvantages. Integer N is a simple architecture, which fails to meet the bandwidth requirement for a specific channel spacing.[1] Furthermore, the output frequency changes only by integer multiples of the reference. Fractional N offers fine resolution, increased loop bandwidth, and lower phase noise. The main disadvantage is the poor fractional spurious performance at the output of the synthesizer. $\Delta\Sigma$ fractional N architecture offers reduced impact of spurious frequencies compared with fractional N and faster settling time compared with integer N for the same frequency resolution.[2,3] However, to sufficiently filter out the quantization noise, the loop bandwidth cannot be too wide, or a quantization noise suppression technique should be used.[4–6]

A topology, which offers comparable performance to $\Delta\Sigma$ fractional N architecture without suffering from quantization noise, is the dual-loop architecture, incorporating simple digital circuitry and prescalers with reduced range of division ratios. Recently, the dual-loop synthesizer configurations have gained renewed interest.[7–9] Not only they can satisfy both speed and bandwidth requirements, but also the integration advancements lead to smaller areas, while at the same time recent circuit design approaches[10] result in low power consumption.

The two loops can be combined in serial or parallel arrangement as shown in Figs. 1(a) and 1(b), respectively.[7,8] A single sideband (SSB) mixer connecting the loops is placed either within one of the loops (serial-connection) or at the output of the two loops (parallel-connection). The parallel-connection offers faster settling time while the serial one offers lower noise level. In the rest of the paper, we will refer to arrangement 1(a) as the classical serial-connected topology.

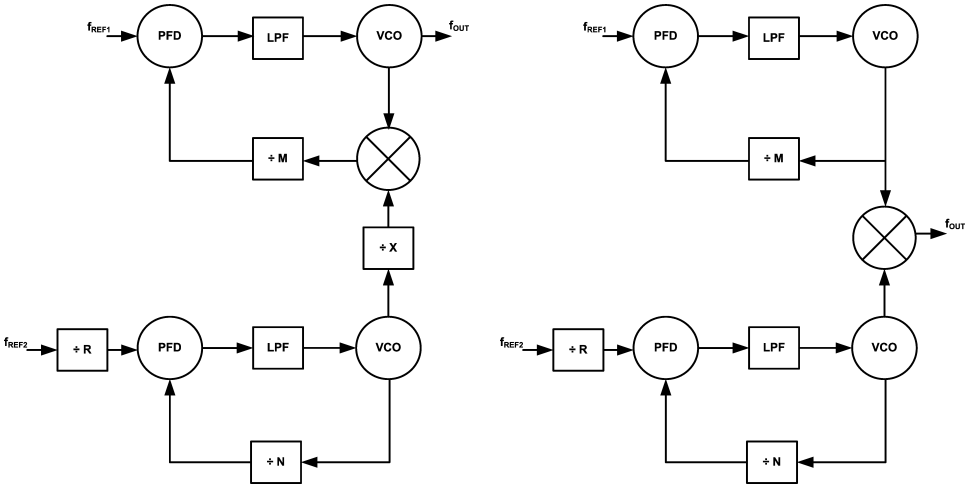

Fig. 1. (a) Serial- and (b) parallel-connected dual-loop architectures.

The main objective of this work is to demonstrate that the proposed modified dual-loop architecture can offer lower phase noise levels than integer N and classical dual-loop architectures. We focus on dual-loop topologies and propose a modified serial-connected architecture, where the divider of the upper (high-frequency) loop is placed right after the VCO and before the mixer. Moving the divider of the classical serial dual-loop synthesizer in the loop, the division ratio becomes much smaller contributing less phase noise in the overall resulting system as will be seen in the analysis and measurements below. Now, the mixer must be designed at a lower frequency, while signals of comparable frequencies feed both the RF and LO ports. The divider attenuates the sidebands resulting from the VCO of the upper loop, before the high-frequency signal drive the mixer. Thus, the harmonic intermodulation distortion is effectively reduced. Furthermore, an additional low-pass filter is inserted at the output of the mixer to provide further attenuation of the higher-order products of the mixer.

In Sec. 2, we present in detail the proposed architecture, Sec. 3 gives the theoretical aspects for contribution on phase noise of the system components, while Sec. 4 provides the estimated overall phase noise and outlines the implementation and measurement results. Finally, some conclusions are outlined in Sec. 5.

2. Architecture

The frequency synthesizer for our application generates signals in the frequency range 4850–5050 MHz, with a channel spacing of 10 MHz. Typical phase noise values of -100 dBc/Hz and approximately -120 dBc/Hz, respectively, at 1 MHz and 10 MHz frequency offsets are required to accommodate for modulations of high spectral efficiency (16-QAM, 64-QAM) used in modern WLAN.[11–14]

The block diagram of the proposed synthesizer is presented in Fig. 2. A dual-loop architecture is employed in order to achieve finer resolution without limiting the bandwidth, and therefore, the locking speed of the synthesizer. The main advantage of the dual-loop architecture is that it can meet both the specifications for phase noise and resolution, by maintaining the large bandwidth of the high-frequency loop and the small reference frequency of the lower loop.[7,15] Furthermore, a lower frequency division ratio is achieved, thus improving the frequency divider complexity.

In the architecture presented above, the output frequency of the synthesizer is calculated as

$$f_{\mathrm{OUT}} = f_{\mathrm{OFFSET}} + N \cdot f_{\mathrm{CHANNEL}} = M \cdot f_{\mathrm{REF1}} + N \cdot \left(\frac{M}{R \cdot X} \cdot f_{\mathrm{REF2}} \right). \qquad (1)$$

The upper loop of the synthesizer provides a large frequency offset f_{OFFSET}, while the lower loop defines the resolution of the synthesizer f_{CHANNEL}.[16] The two loops are combined in series, through a mixer, placed within the upper loop. Thus, the sidebands generated at the output of the highly nonlinear mixer are suppressed by the low-pass filter placed at the output of the mixer.

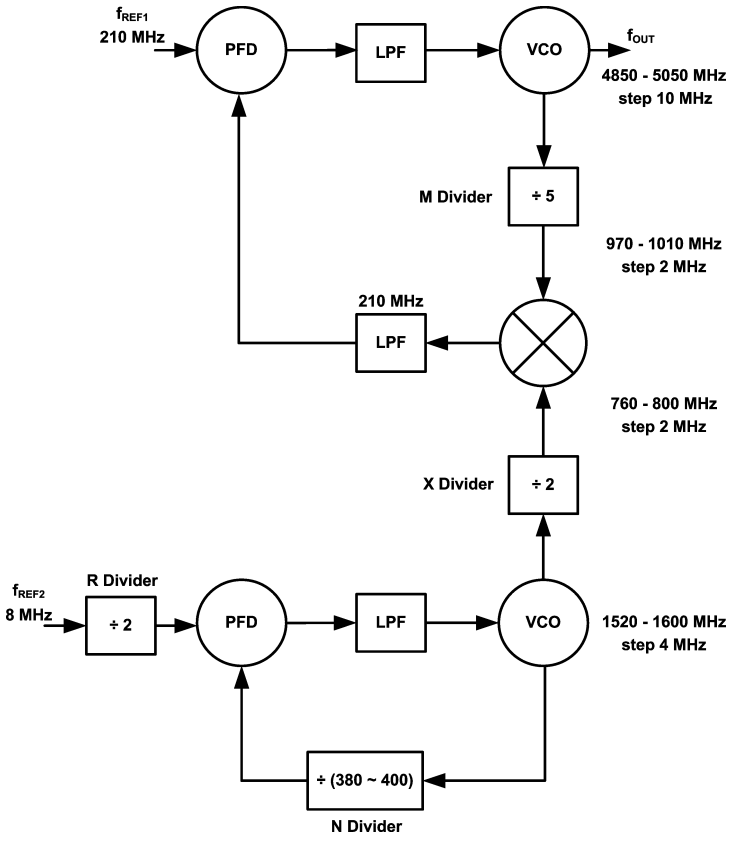

Fig. 2. The proposed dual-loop architecture.

In contrast to other dual-loop architectures reported (see Refs. 7–9 and 16), the M-divider of the upper loop is placed before the mixer, thus attenuating the sidebands produced at the output of the VCO and reducing the phase noise injected in the high-frequency drive of the mixer. Finally, the X prescaler allows for an increase in the resolution of the lower-frequency loop without reducing the reference frequency of the lower loop.

Considering the integration aspects, care must be taken in the power-hungry blocks of a dual-loop architecture which apart from the VCO are the high-frequency divider, following the VCO, and the mixer. Compared to other dual-loop architectures, it is advantageous to implement a lower-frequency mixer (simple topologies, low power consumption). Furthermore, using recent techniques like a true-single-phase-clock divider[10] could result in a very low consumption, small die area, high-frequency divider following the VCO. In addition, such divider can be driven directly by the output of the VCO eliminating the need for a driver stage.

Finally, the output of the low-frequency loop (1520–1600 MHz) can be mixed with the output of the X divider (760–800 MHz) to produce along with f_{out}

(4850–5050 MHz) the frequency band used in the WLAN 802.11a/b/g standard. Hence, this architecture can be directly applied in multistandard transceivers.

3. Modeling of the System and Phase Noise Analysis

Given the basic electronic elements (VCO, phase detector), the loop filters of the two loops determine the settling time, phase noise, and spurious levels at the output of the synthesizer. Therefore, their design is of crucial importance to the behavior of the synthesizer.

To determine the overall phase noise, we calculate the phase noise contribution of each component separately. The linear model[17] of the high-frequency loop including the main phase noise contributors (as presented in Fig. 3), is suitable both for deriving the open- and closed-loop gain of the loop, and for modeling the noise behavior of all the individual blocks. After some mathematical manipulation, we get the transfer functions of individual system components (VCO, PD, etc.) as presented in Table 1.

Oscillators are responsible for a considerable part of phase noise present at the output of the synthesizer, as they tend to convert perturbations from any source into phase variation, amplified at their output. However, the phase-frequency detector and the frequency dividers also contribute to the overall output noise, and will be therefore, taken into account when estimating the synthesizer overall output noise. Since $F(s)$ is either unity or a low-pass transfer function, the PLL operates as a low-pass filter for phase noise arising in the reference signal and as high-pass filter for phase noise originating in the VCO.

Also, the loop acts as a low-pass filter to the phase noise contributed by the phase-frequency detector and the frequency divider.[18] The divider and detector

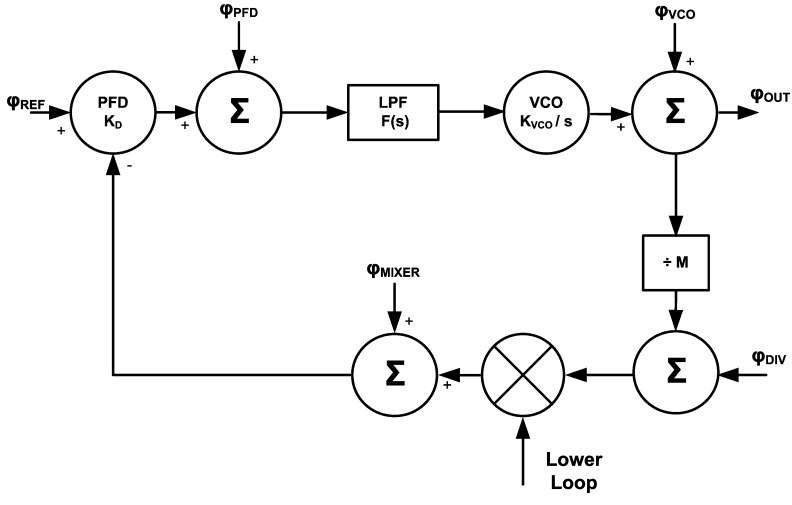

Fig. 3. High-frequency loop linear model.

Table 1. Transfer functions for various noise sources.

Noise source	Transfer function
TCXO	$\dfrac{K_{\mathrm{VCO}} \cdot K_D \cdot F(s)}{s + K_{\mathrm{VCO}} \cdot K_D \cdot F(s)/M}$
Divider	$\dfrac{K_{\mathrm{VCO}} \cdot K_D \cdot F(s)}{s + K_{\mathrm{VCO}} \cdot K_D \cdot F(s)/M}$
PFD	$\dfrac{K_{\mathrm{VCO}} \cdot F(s)}{s + K_{\mathrm{VCO}} \cdot K_D \cdot F(s)/M}$
VCO	$\dfrac{s}{s + K_{\mathrm{VCO}} \cdot K_D \cdot F(s)/M}$
Mixer	$\dfrac{K_{\mathrm{VCO}} \cdot K_D \cdot F(s)}{s + K_{\mathrm{VCO}} \cdot K_D \cdot F(s)/M}$

amplify the contributed phase noise at the output by the factor M and K_D/M, respectively. From all the above, reduced phase noise demands contradictory bandwidth requirements regarding the VCO contribution and the contribution of the rest of the loop components. Figure 4 shows the phase noise contribution of the various noise sources of the synthesizer (multiplied by the corresponding transfer function).

To get the expression for the overall output phase noise, the phase noise of the low-frequency loop $\mathsf{L}_{\mathrm{LL}}(s)$, is added (through the mixer transfer function) to the

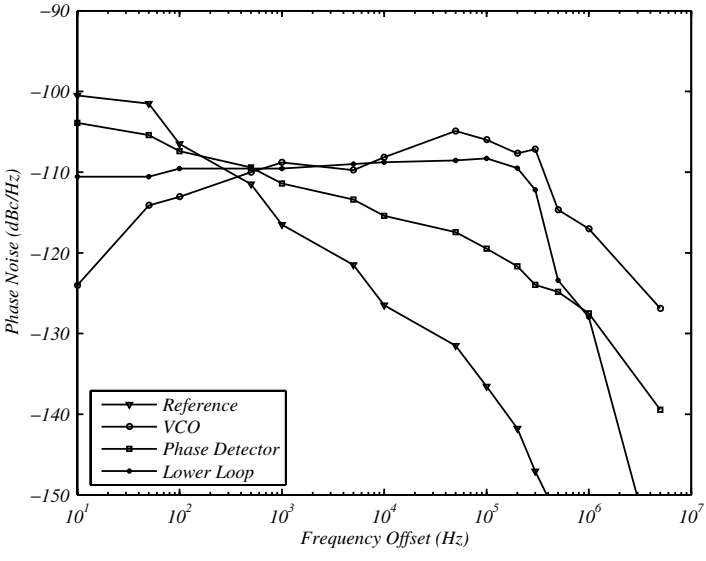

Fig. 4. Phase noise contribution of the various noise sources.

phase noise contributed by the rest of the components of the upper loop:

$$\mathsf{L}_{\mathrm{TOTAL}}(s) = \mathsf{L}_{\mathrm{VCO}}(s)|1 - H(s)|^2 + M^2\mathsf{L}_{\mathrm{REF}}(s)|H(s)|^2 + \mathsf{L}_{\mathrm{PFD}}(s)\frac{M^2}{|K_{\mathrm{PFD}}|^2}|H(s)|^2 + M^2\mathsf{L}_{\mathrm{LL}}(s)|H(s)|^2. \quad (2)$$

The calculated phase noise of the dual-loop synthesizer, shown in Fig. 2, is compared with the calculated phase noise at the output of a hypothetical single-loop synthesizer. The latter produces the same range of output frequencies as the dual-loop synthesizer, with an equal channel spacing (10 MHz) using an f_{REF} of 10 MHz and a divider of 485–505. Figure 5 shows the calculated phase noise of the proposed architecture, the phase noise of the single loop (using the same loop filter), and the phase noise of the optimized single loop (optimum loop filter). The phase noise of the single loop is clearly worse than the calculated phase noise of the dual-loop design both at low- and high-frequency offsets, justifying the choice of a dual-loop architecture for our application. Regardless of the implementation approach (discreet or IC) the dual-loop synthesizer will always present lower phase noise levels than integer N. Therefore, even for integrated solutions with considerably low phase noise levels[13,14] the corresponding dual-loop is expected to perform even better.

Furthermore, the classical serial dual-loop topology (Fig. 1(a)) was investigated by designing a synthesizer with the same requirements as the proposed, using similar electronic components. Table 2 shows the values of the parameters of this synthesizer.

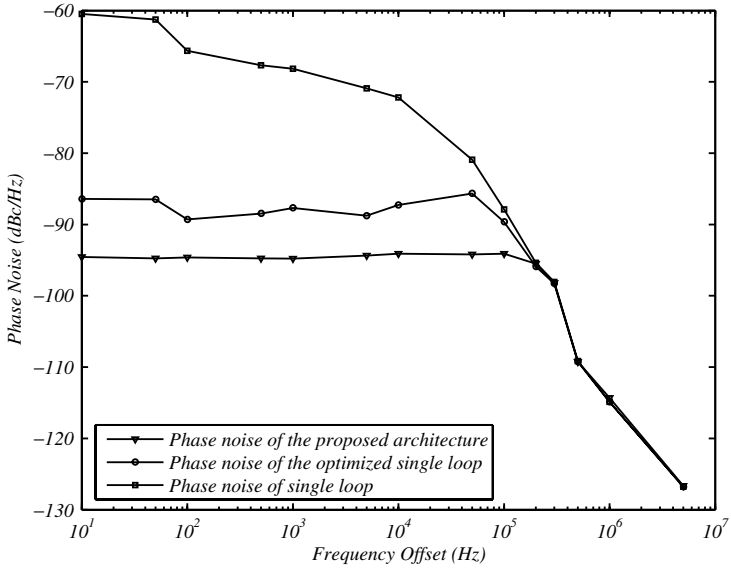

Fig. 5. Calculation of the overall output phase noise of the proposed topology, the single loop, and the optimized single loop.

In the classical serial dual loop the divider is connected at the output of the mixer and the division ratio M does not affect the phase noise contribution $\mathsf{L}_{\mathrm{LL}}(s)$ of the lower loop. However, as the value of M for the classical serial dual loop must be several times higher than the one in the proposed architecture, the resulting overall phase noise will be higher because the M^2 term appears in all phase noise components except that of the VCO. As seen in Table 2, the value of M for the classical dual-loop architecture is five times higher than the one in the proposed system.

Figure 6 illustrates the calculated overall phase noise for the classical serial-connected along with the one corresponding to the proposed topology. From this figure, it can be concluded that the proposed synthesizer exhibits considerable improvement in phase noise.

Table 2. System characteristics for the classical serial-connected topology.

f_{REF1}	210 MHz
f_{REF2}	40 MHz
M	20
N	65–85
X	2
R	2
Upper loop VCO	4850–5050 MHz
Lower loop VCO	1300–1700 MHz

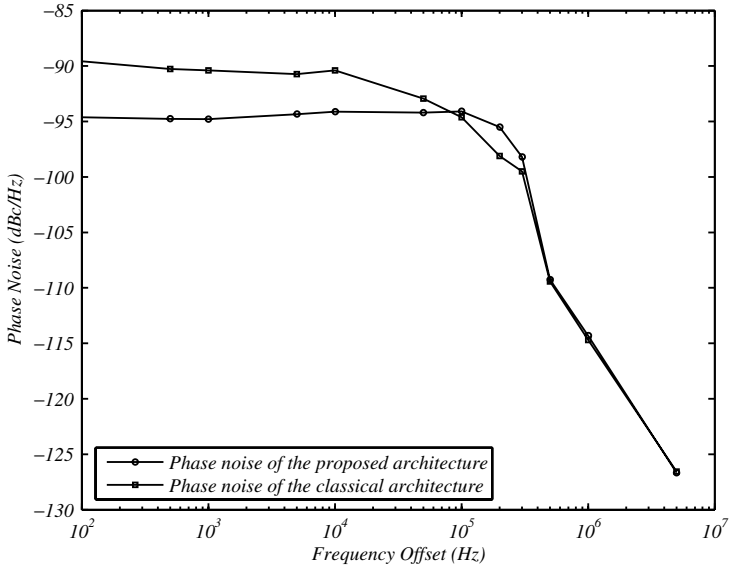

Fig. 6. Calculation of the overall output phase noise of the classical serial-connected and the proposed topology.

4. System Implementation and Measurements

To verify our considerations, a synthesizer at 5 GHz was built using discrete components to implement the upper- and lower-frequency loops. This provides flexibility for fine-tuning and fast prototype implementation. The low-frequency VCO generates signals in the frequency range of 1520 MHz to 1600 MHz with a 4 MHz step. The output of the lower loop is divided by $X = 2$ to produce the LO input frequency of the mixer. The high-frequency VCO output, ranging from 4850 MHz to 5050 MHz with a 10 MHz step, is divided by $M = 5$ and then down-converted by the LO signal to produce an IF signal of 210 MHz. The active filter used at the high-frequency loop and the third-order filter used at the low-frequency loop are shown in Figs. 7(a) and 7(b), respectively. The corresponding bandwidths for the two loops are 500 KHz (high-frequency loop) and 200 KHz (low-frequency loop).

The output power spectrum and the phase noise of the implemented synthesizer were measured by directly connecting it to a spectrum analyzer with phase noise measurement capabilities. Figure 8 illustrates the measured phase noise at the output of the synthesizer showing -100 dBc/Hz at 300 kHz offset and -115 dBc/Hz at 1 MHz offset, whereas the plot shown in Fig. 9 shows the output spectrum indicating an output power of -7.5 dBm. The spurious levels are -118 dBc and -123 dBc at 8 MHz and 210 MHz frequency offsets, respectively.

In addition, Fig. 10 shows a comparison between measured and calculated — using MATLAB — results. It must be noted that the latter corresponds to an ideal system without any losses or mismatches, whereas the implemented system exhibits implementation losses. Considering the above measured and calculated results in Fig. 10, they are in very good agreement.

The prototype was implemented only to confirm the phase noise properties of the proposed architecture. The resulting advantage is due to the different arrangement of the circuit elements in the system architecture. Therefore, it is expected that the phase noise of the proposed architecture will always be lower even when the system is implemented in integrated form.

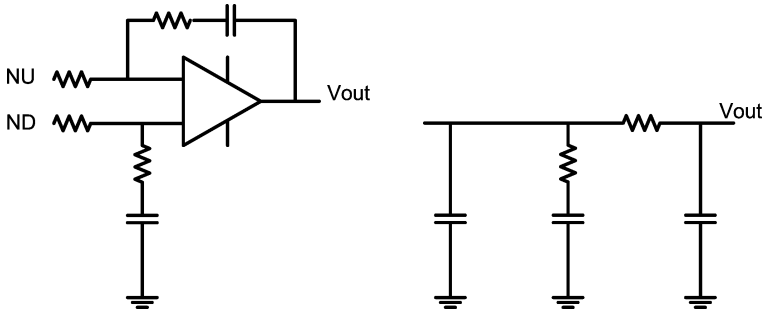

Fig. 7. Loop filters of the (a) high and (b) low frequency loop.

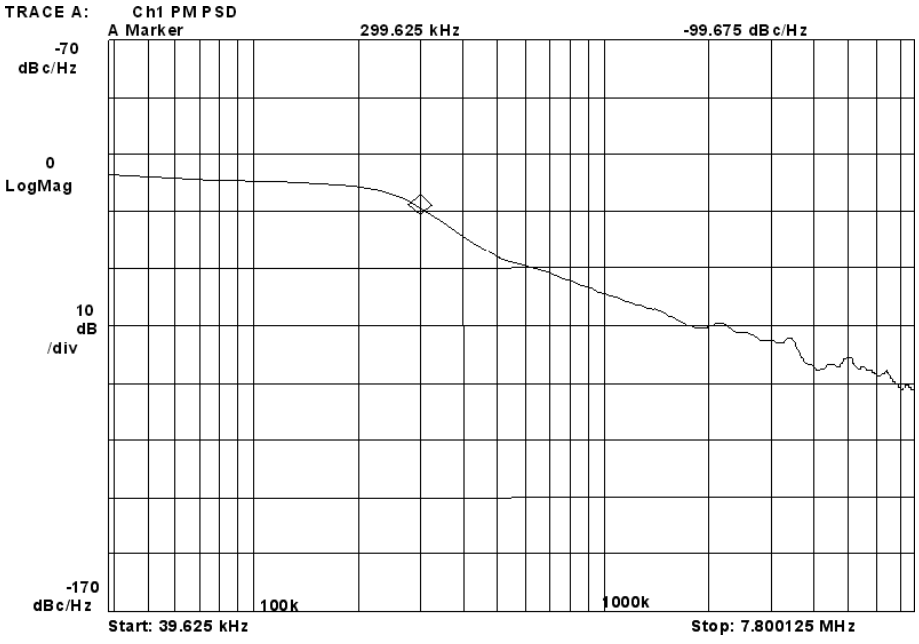

Fig. 8. Measurement of the phase noise.

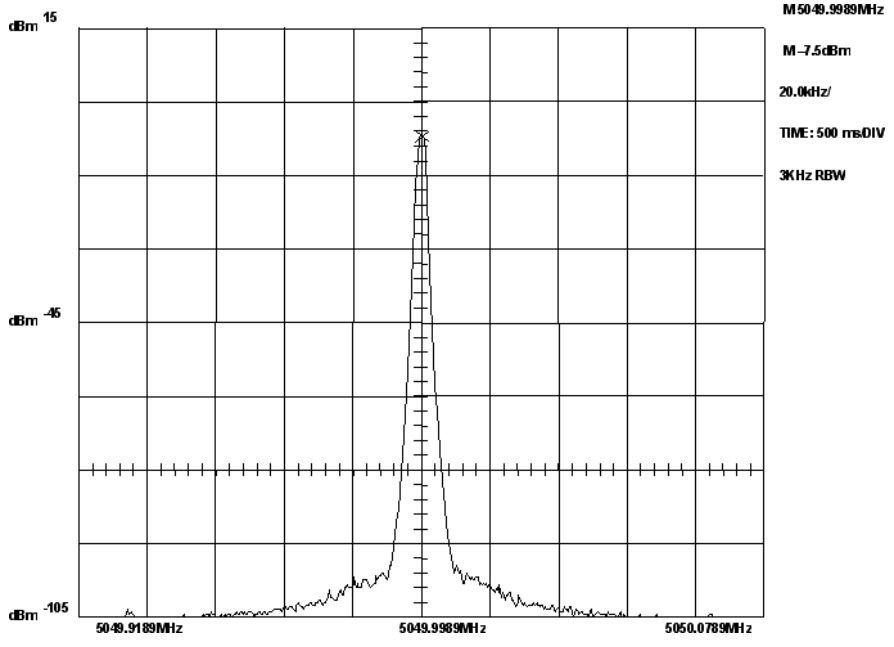

Fig. 9. Measurement of the output spectrum.

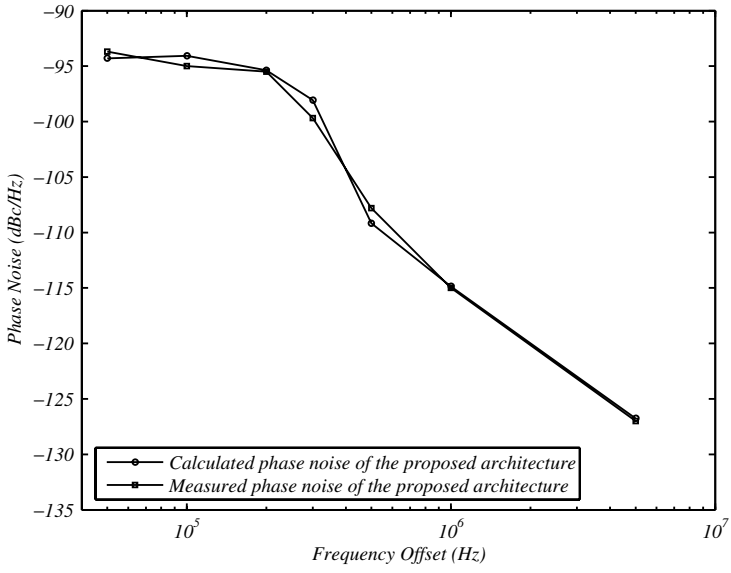

Fig. 10. Phase noise measurement and calculated results.

5. Conclusions

In this paper, a modified dual-loop synthesizer architecture is proposed for WLAN applications at 5 GHz. The dual-loop architecture achieves both good resolution and low phase noise over a wide bandwidth and is thus suitable for 802.11a applications. Due to the broadband requirements for such systems, emphasis is given to phase noise performance. Phase noise analysis is presented and the overall system phase noise is estimated. In addition, it is shown that this architecture exhibits lower phase noise when compared to recently reported dual-loop configurations. To demonstrate the noise characteristics of the synthesizer, a prototype using discrete components was built and tested. According to the measurements, the synthesizer achieves a phase noise of -100 dBc/Hz and -115 dBc/Hz at 300 kHz and 1 MHz offsets, respectively, and an output power level of -7.5 dBm. The measured phase noise is satisfactory for system integration in 5 GHz WLAN transceivers.

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