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A 5-GHz INJECTION-LOCKED PHASE-LOCKED LOOP

Fotis Plessas and Grigorios Kalivas
Department of Electrical and Computer Engineering
University of Patras
Rion 26500, Greece

Received 21 December 2004

ABSTRACT: *In this paper, we introduce a 5-GHz injection-locked phase-locked loop (ILPLL). A new method is presented for accurate analysis of the phase-noise performance of the proposed system. Furthermore, comparison with other phase-noise-estimation techniques demonstrates that our method provides an accurate characterization of any ILPLL topology. The theoretical and calculation results show an improved performance for phase noise, locking range, and power consumption compared to conventional phase-locked loops (PLLs) and injection-locked oscillators (ILOs). Furthermore, we demonstrate the pulling behavior of the injected oscillator and examine the obtained results. To verify the presented analysis, a 5-GHz prototype has been implemented, which achieves −119-dBc/Hz at 100-KHz frequency offset, producing +4.5 dBm of output power and consuming 9 mA at 3 V.* © 2005 Wiley Periodicals, Inc. Microwave Opt Technol Lett 46: 80–84, 2005; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.20907

Key words: *frequency synthesizer; injection-locked oscillator; injection-locked phase-locked loop; locking range; phase noise; transfer function; voltage-controlled oscillator*

1. INTRODUCTION

A promising technique for realizing low-phase-noise levels and increased locking range is the injection-locked phase-locked loop (ILPLL). Studied by several authors [1–5], this method is a combination of a PLL and an ILO. The voltage-controlled oscillator (VCO) of such a loop is an injected oscillator [6–9], in contrast to the free-running oscillator of conventional PLLs. A microwave oscillator can be synchronized to an external low-power stable signal, thus providing a low-phase-noise high-power output.

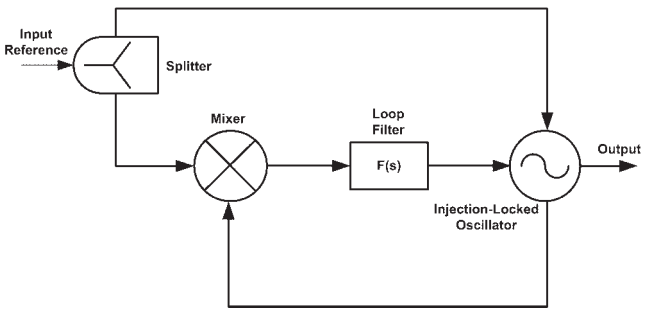

Figure 1 Injection-locked synthesizer

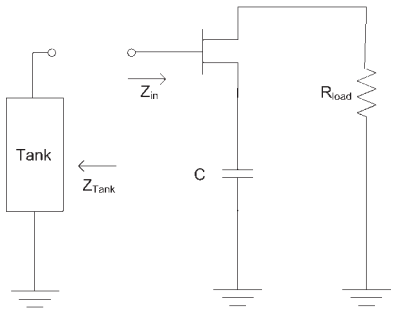

Figure 2 Common-source capacitive feedback oscillator

The input reference signal is divided into two parts using a power splitter. One part is used to provide the reference signal to the mixer, which acts like a phase detector, whereas the other part is injected into the VCO. The mixer produces a phase-error signal that is processed by the loop filter and tunes the VCO.

Huang [1] reported the nonlinear analysis of a MESFET injection locked oscillator at 2.7 GHz, whereas Razavi [2] presented the injection-pulling phenomena of a 1-GHz phase-locked oscillator. Optically injected and phase-locked combined systems have been extensively reviewed by Blanchflower [2] and Ramos [3]. Finally, a 10-GHz injection-locked phase-locked oscillator was analyzed and demonstrated in [5], where the same device is used as both phase detector and oscillator.

In this paper, we develop a different approach for ILPLL design at 5 GHz by applying a technique used in optical communications [3, 4]. The proposed system, as shown in Figure 1, is suitable for synthesizer applications at 5 GHz due to its implementation characteristics. Furthermore, we newly address the phase-noise analysis of ILPLLs using the loop linear model and compare the results with previously reported work. The analytical expression for the locking range is also derived and the pulling behavior of the injected oscillator is demonstrated.

For the experimental investigation, a prototype was implemented using commercial components. The measurement results illustrate the capability of the proposed analysis to accurately predict the phase-noise performance, demonstrate the main characteristics, and confirm the feasibility of the system.

The contents of this paper are as follows. In section 2, we present the design and synchronization of the oscillator, which is one of the most critical parts of the proposed circuit. The phase-noise model and locking-range analysis are then proposed in section 3. Section 4 reports the implementation and experimental results, while the conclusions are presented in section 5.

2. DESIGN AND SYNCHRONIZATION OF THE OSCILLATOR

2.1. The Oscillator

A common-source capacitive feedback oscillator, illustrated in Figure 2, is employed by using a GaAs Hetero-Junction FET with a parallel resonant applied at the gate.

The equivalent circuit of the tank, which consists of a hyperabrupt GaAs tuning varactor (with γ equal to 1.25) and an inductor, is shown in Figure 3. $C_s(V)$ is the variable capacitor, C_p and L_s are the parasitic capacitor and inductor, respectively, and $R_s(V)$ is the voltage-dependent resistor. Finally, L is the external inductor. The tuning voltage V can vary from 0 to 7 V.

Initially, the unstable condition

$$R_{\tan k} + R_{in} < 0 \tag{1}$$

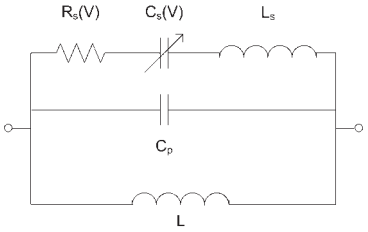

Figure 3 Equivalent circuit of the parallel tank

is observed. Then R_{in} becomes less negative until

$$R_{\tan k} + R_{in} = 0, \tag{2}$$

$$X_{\tan k} + X_{in} = 0, \tag{3}$$

which are the conditions for stable oscillation.

Both transient and harmonic-balance analyses are used to obtain the performance of the oscillator. The tuning range of the oscillator is 310 MHz (4770 to 5080 MHz), thus giving +5 dBm of output power.

2.2. Synchronization

The phase noise of the ILO is given by [1]:

$$\mathscr{L}_{\mathrm{ILO}}(\omega)=\frac{\left(\frac{\omega_{\mathrm{O}}}{2\mathrm{Q}}\frac{\mathrm{V_{REF}}}{\mathrm{V_O}}\right)^2\mathscr{L}_{\mathrm{REF}}\cos^2\varphi+\omega^2\mathscr{L}_{\mathrm{VCO}}}{\left(\frac{\omega_{\mathrm{O}}}{2\mathrm{Q}}\frac{\mathrm{V_{REF}}}{\mathrm{V_O}}\right)^2\cos^2\varphi+\omega^2}, \tag{4a}$$

$$\varphi = \theta_{inj} - \theta_o, \tag{4b}$$

where φ is the stationary phase difference between the free-running oscillator and the reference signal, ω is the offset carrier frequency, V_{REF}, V_O, ω_O, and Q, are the voltage of the reference signal, the voltage of the free-running signal, the free-running frequency, and the quality factor of the embedding network, respectively. $\mathscr{L}_{\mathrm{VCO}}$ is the single-sideband spectral density of the phase noise of the free-running oscillator and $\mathscr{L}_{\mathrm{REF}}$ is the single-sideband spectral density of the phase noise of the reference signal. φ is expressed as [7]:

$$\sin\varphi = 2Q\frac{\omega_O - \omega_{REF}}{\omega_O}\frac{V_O}{V_{REF}}, \tag{5}$$

where ω_{REF} is the reference frequency.

3. LOCKING RANGE AND PHASE-NOISE ANALYSIS

3.1. Locking Range

When the VCO (using the ILO mechanism) is locked onto the reference, we obtain

$$\omega_{inj} = \omega_o - \Delta\omega_{ilo}\sin(\theta_{inj} - \theta_o), \tag{6}$$

where

$$\Delta\omega_{ilo} = \frac{\omega_O}{2Q}\frac{V_{inj}}{V_{out}}, \tag{7}$$

ω_{inj} and θ_{inj} are the frequency and phase of the reference, whereas ω_o and θ_o are the frequency and phase of the free-running VCO, respectively. Moreover, in a PLL with ω_{inj} as a reference, the well-known equation for the PLL becomes

$$\omega_{inj} = \omega_o + \Delta\omega_{pll}\cos(\theta_{inj} - \theta_o + \varphi_T), \tag{8}$$

where φ_T is the phase shift around the loop and

$$\Delta\omega_{pll} = K_{VCO}K_{PD}K_{LF}. \tag{9}$$

If we incorporate the injection-locked oscillator into a PLL, the term ω_o in Eq. (8) represents ω_{inj}, as expressed in Eq. (6). The new phase equation becomes

$$\omega_{inj} = \omega_o + \Delta\omega_{ilpll}\sin(\theta_{inj} - \theta_o + \psi), \tag{10}$$

where

$$\Delta\omega_{ilpll} = \sqrt{\Delta\omega_{pll}^2 + \Delta\omega_{ilo}^2 + 2\Delta\omega_{pll}\Delta\omega_{ilo}\sin\varphi} \tag{11}$$

and

$$\tan\psi = -\frac{\Delta\omega_{pll}\cos\varphi}{\Delta\omega_{pll}\sin\varphi + \Delta\omega_{ilo}}. \tag{12}$$

Eq. (10) is the equivalent Adler's equation for the proposed system. An increased locking-range is obtained, which is larger than that of a conventional PLL.

The numerical results obtained using Eq. (11) are plotted in Figure 4. The locking range of a conventional PLL using the same VCO and phase detector is 18.8 MHz, whereas the locking range of the ILPLL with −25-dBm injected power is 20.4 and 26.1 MHz for $\varphi = 0°$ and $\varphi = 90°$, respectively. For injected-power levels higher than −15 dBm, the locking range of the ILPLL is more than twice that of a conventional PLL.

3.2. Phase-Noise Analysis

Let us consider the loop linear model, as shown in Figure 5, where K_{VCO} and K_{PD} are the VCO and phase-detector gains, respectively, and $F(s)$ is the transfer function of the loop filter. The basic components of the loop (injection-locked oscillator, phase detec-

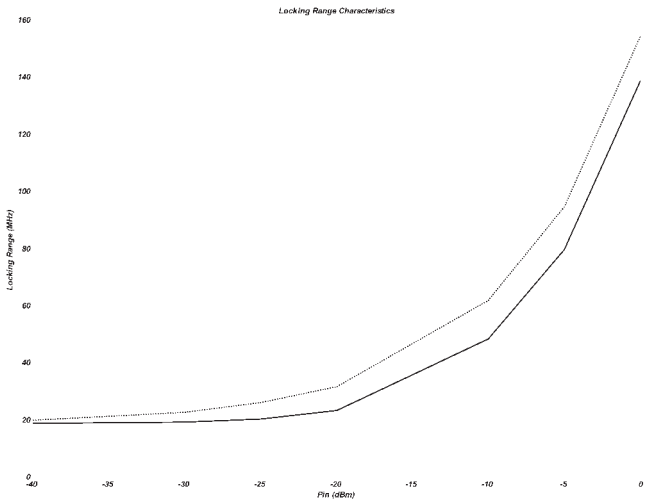

Figure 4 Locking-range characteristics of the injection-locked PLL

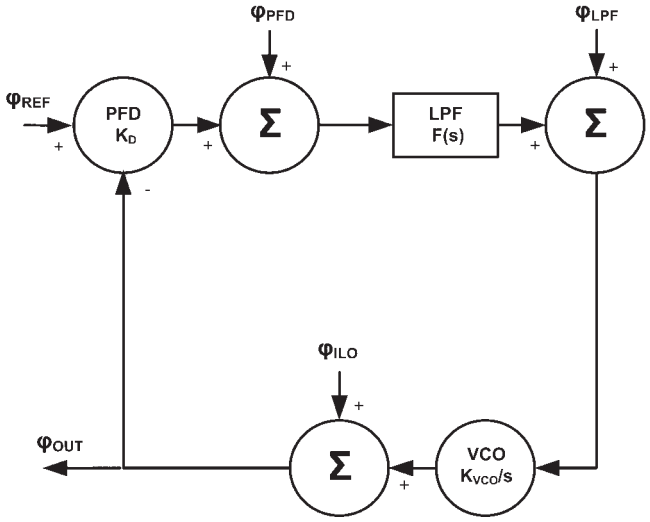

Figure 5 Noise model

tor, and loop filter) are assumed to be perfect, noise-free components, followed by a source that introduces noise (φ_{ILO}, φ_{PFD}, and φ_{LPF}).

If we apply the phase-locked-loop technique to an injection-locked oscillator, the total output phase noise of the loop is given by

$$\varphi_{OUT} = \{1 - H(s)\}\varphi_{ILO} + \frac{1}{K_{PFD}} H(s)\varphi_{PFD} + H(s)\varphi_{REF} + \frac{1}{F(s)\,K_{PFD}} H(s)\varphi_{LPF}, \quad (13)$$

where

$$G(s) = K_{PFD}\frac{K_{VCO}}{s}F(s) \quad \text{and} \quad H(s) = \frac{G(s)}{1 + G(s)}.$$

Taking into account that $\mathscr{L}_{\mathrm{ILO}}(\omega)$, $\mathscr{L}_{\mathrm{PFD}}(\omega)$, $\mathscr{L}_{\mathrm{REF}}(\omega)$, and $\mathscr{L}_{\mathrm{LPF}}(\omega)$ are the single-sideband spectral densities of the noise terms φ_{ILO}, φ_{PFD}, φ_{REF}, and φ_{LPF}, respectively (in units of

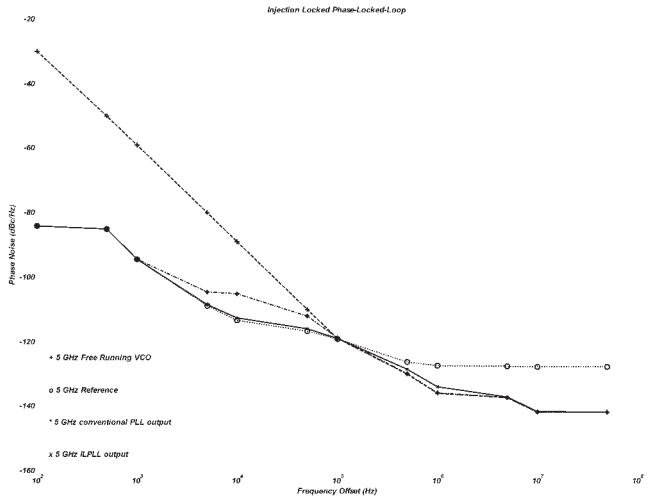

Figure 6 Output phase noise of the proposed ILPLL and a conventional PLL with the same loop filter, reference, and VCO

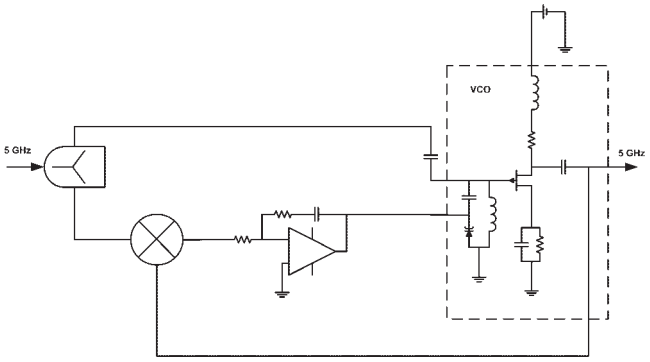

Figure 7 The implemented ILPLL

rad^2/Hz), the total spectral density of the phase noise of the loop, $\mathscr{L}_{\mathrm{OUT}}(\omega)$, is given by

$$\mathscr{L}_{\mathrm{OUT}}(\omega) = \mathscr{L}_{\mathrm{ILO}}(\omega)|1 - \mathrm{H}(\omega)|^2 + \mathscr{L}_{\mathrm{PFD}}(\omega)\frac{1}{|\mathrm{K_{PFD}}|^2}|\mathrm{H}(\omega)|^2 + \mathscr{L}_{\mathrm{REF}}(\omega)|\mathrm{H}(\omega)|^2 + \mathscr{L}_{\mathrm{LPF}}(\omega)\frac{1}{|\mathrm{K_{PFD}F}(\omega)|^2}|\mathrm{H}(\omega)|^2. \quad (14)$$

When Eq. (4a) is substituted into Eq. (14), the output phase noise of the loop becomes

$$\mathscr{L}_{\mathrm{OUT}}(\omega) = \frac{\left(\frac{\omega_{\mathrm{O}}}{2\mathrm{Q}}\frac{\mathrm{V_{REF}}}{\mathrm{V_O}}\right)^2 \mathscr{L}_{\mathrm{REF}}\cos^2\varphi}{\left(\frac{\omega_O}{2Q}\frac{V_{REF}}{V_O}\right)^2\cos^2\varphi + \omega^2}|1 - H(\omega)|^2 + \frac{\omega^2\mathscr{L}_{\mathrm{VCO}}}{\left(\frac{\omega_{\mathrm{O}}}{2\mathrm{Q}}\frac{\mathrm{V_{REF}}}{\mathrm{V_O}}\right)^2\cos^2\varphi + \omega^2}|1 - H(\omega)|^2 + \mathscr{L}_{\mathrm{REF}}(\omega)|\mathrm{H}(\omega)|^2, \quad (15)$$

where the effect of $\mathscr{L}_{\mathrm{PFD}}(\omega)$ and $\mathscr{L}_{\mathrm{LPF}}(\omega)$ is not significant enough and have been neglected.

The filter is an active integrator with the following transfer function:

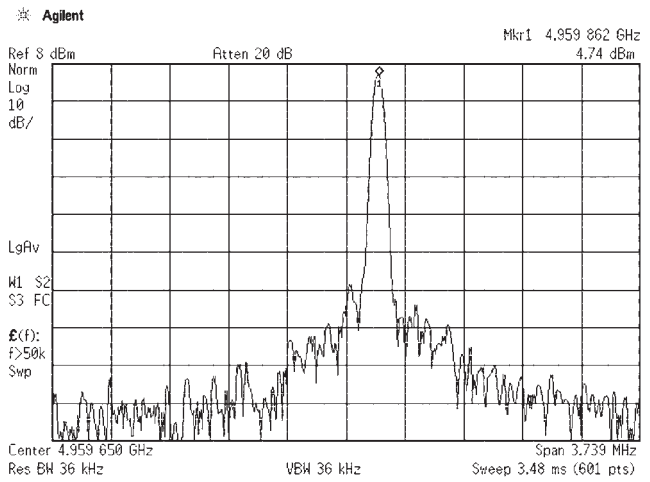

Figure 8 Output spectrum of the free-running VCO

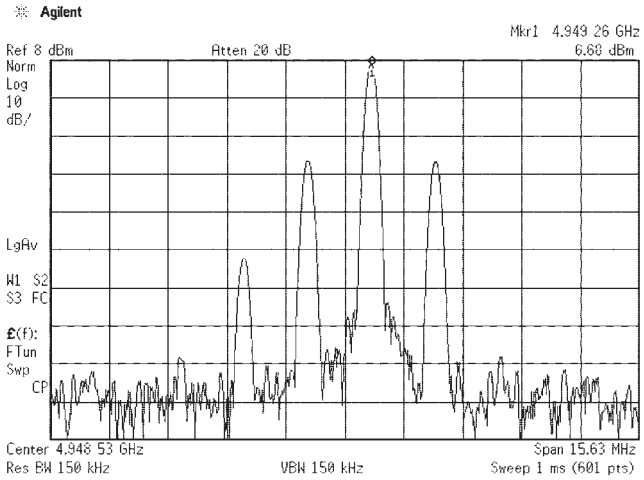

Figure 9 Measured spectrum of the free-running oscillator under injection

$$F(s) = \frac{s\tau_2 + 1}{s\tau_1},\ \tau_1 = R_1C,\ \tau_2 = R_2C. \tag{16}$$

Computing the overall output phase noise of the proposed system according to Eq. (15), we obtain the results shown in Figure 6.

It should be noted that the ILPLL has a 10-dB lower phase noise level at 10-KHz offset from the carrier, as compared to the conventional PLL. The phase-noise improvement can become more significant for integrated (SiGe or CMOS) VCOs. In this case, even 20-dB reduction of in-band phase noise can be achieved, compared to that of a wider loop-bandwidth conventional PLL.

A different way of analyzing subharmonic ILPLLs was proposed by Sturzebecher [10], who applied injection locking to a PLL oscillator. We modify the analysis in [10] to suit the fundamental mode (and not the subharmonic used there) of operation, and apply it in our ILPLL. The numerical results we obtain are similar to the results produced by our analysis. These results support the proposed analysis, which constitute an accurate method for the phase-noise characterization of any ILPLL topology. As shown in the next section, the analysis is also validated by the measured data.

4. IMPLEMENTATION AND MEASUREMENTS

To demonstrate the feasibility of the proposed ILPLL and verify the analysis outlined in the previous section, the system shown in

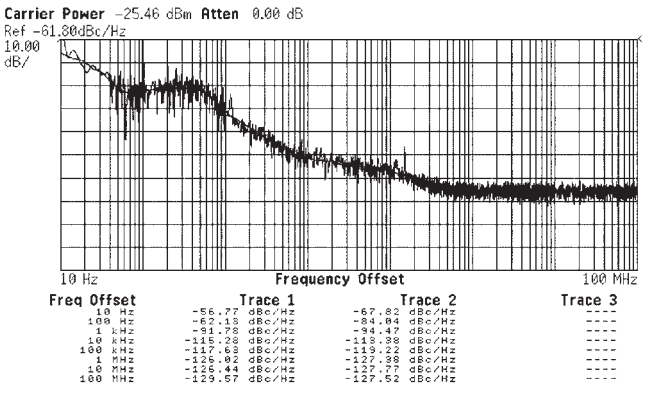

Figure 10 Phase-noise measurement of the reference

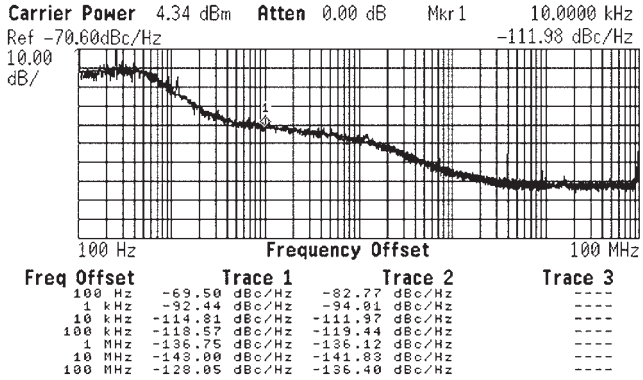

Figure 11 Phase-noise measurement of the ILPLL

Figure 7 was designed and implemented. For the implementation, a PTFE substrate with ε_r of 6.15 and thickness of 10 mils was used. Impedance matching is achieved by using distributed microstrip-line elements. The prototype dissipates by 27 mW at 3 V.

4.1. The Oscillator

The custom-designed VCO, shown within the dashed-line box in Figure 7, was first implemented and tested. A low-noise GaAS HeteroJunction FET and an hyperabrupt GaAs tuning varactor were used, as described in section 2. The resulting measured K_{VCO} was 47 MHz/V. Figure 8 shows the spectrum of the free-running oscillator at 4959 MHz producing +4.73 dBm of output power.

Figure 9 illustrates the output spectrum of an injection-pulled oscillator, when ω_{inj} is outside the locking range. Razavi studied the pulling behavior of an injection-locked oscillator and arrived at a similar result in [2]. The injected level is approximately 30-dB below the output power level. ω_{inj} is the right-hand spectral line (above ω_0). The peak value is at $\omega_{inj} - \omega_b$, where $\omega_b = \sqrt{(\omega_0 - \omega_{inj})^2 - \omega_L^2}$ and ω_L is the lock range of the injected oscillator. The spectrum contains two more sidebands at $\omega_{inj} - 2\omega_b$ and at $\omega_{inj} - 3\omega_b$.

4.2. The Overall System

The phase-noise performance of the 5-GHz reference source taken directly from a signal generator is shown in Figure 10. The power level of the injected signal is −25.46 dBm in this specific case, whereas power levels down to −33 dBm are adequate for efficient

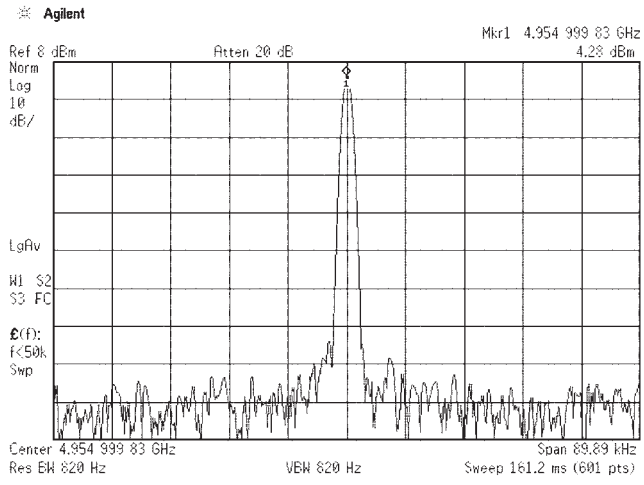

Figure 12 Output spectrum of the ILPLL

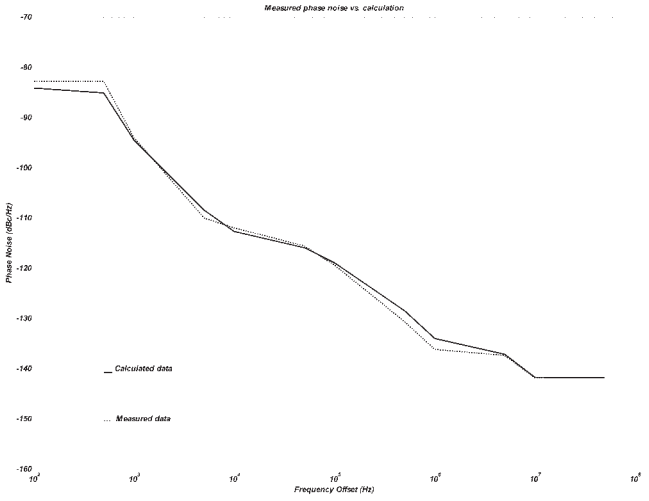

Figure 13 Measurement data superimposed on the calculation results

injection-locking to occur. A 4.5–6-GHz double-balanced mixer is used as phase detector. The measured K_{PD} was 0.4 V/rad.

After the characterization of the phase noise of the reference and the free-running VCO, the overall implemented system was measured. The reference signal and the output of the injected VCO are shaped by the noise-transfer functions and added, as presented in section 3. This results in a total measured output phase noise, as illustrated in Figure 11. As expected, the phase-noise curve follows closely that of the reference for frequency offsets lower than the ILPLL bandwidth. Beyond that point, it reduces further to the level of the VCO noise.

Figure 12 shows the measured output spectrum of the proposed system, when the oscillator injection-locked and phase-locked, and is relatively clean, and the phase noise characterizing the free-running signal has been eliminated.

A comparison of calculated (solid line) and measured (dashed line) phase-noise characteristics of the ILPLL is given in Figure 13. Good agreement between the measured and calculated curves validates the proposed phase-noise analysis.

5. CONCLUSION

In this paper, we have reported an ILPLL suitable for 5-GHz wireless-communication systems. An analytical model was developed and employed to derive the total output phase-noise and locking-range equations. The measurements of the implemented system show that an injected level approximately 30-dB below the output power level is adequate to establish injection locking. The comparison between theory and experiment shows very good agreement.

In operation, the proposed ILPLL achieves a phase noise of −120 dBc/Hz at 1-MHz frequency offset, while consuming 27 mA from a 3-V supply. In contrast to conventional PLLs, the phase-noise performance of the proposed system is significantly better, thus making it suitable for integration in modern LAN receivers.

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InGaP/GaAs HBT POWER AMPLIFIER WITH CMRC STRUCTURE

C. K. Poek, B. P. Yan, and E. S. Yang
Department of Electrical and Electronic Engineering
The University of Hong Kong
Hong Kong SAR, P. R. China

Received 23 December 2004

ABSTRACT: *An InGaP/GaAs heterojunction bipolar transistor (HBT) power amplifier is developed for WCDMA user equipment, specifically, band-1-power class-2 application. The HBT power amplifier demonstrates maximum output power P_{out} of 29.4 dBm and power-added efficiency (PAE) of 48% at a frequency of 1.95 GHz. When operated according to the WCDMA standard, it achieves P_{out} of 27 dBm and PAE of 32.4%. The adjacent channel leakage power ratio (ACLR) is −33 dBc. A compact microstrip resonant cell (CMRC) circuit is implemented on the HBT amplifier in order to further improve the PAE, ACLR, and IM3 performances. This results in improvements of 8 dB and 6% for the ACLR and PAE, respectively.* © 2005 Wiley Periodicals, Inc.
Microwave Opt Technol Lett 46: 84–88, 2005; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.20908

Key words: *compact microstrip resonant cell (CMRC); HBT power amplifier; PAE; ACLR*

1. INTRODUCTION

Current digital mobile-communication systems require high efficiency, high linearity, and low-cost amplifiers for handset transmitters. GaAs-based heterojunction bipolar transistors (HBTs) are a suitable candidate due to their superior power performances. Compared with rival silicon bipolar and GaAs field-effect transistor (FET) devices, HBTs have several advantages, including high linearity, high transconductance, high power added efficiency (PAE), and low $1/f$ noise. These advantages have made GaAs HBTs the preferred technology for many military and commercial applications. High-efficiency HBT MMIC with a PAE of 40% and a P_{out} of 28 dBm [1] and a high-linearity HBT amplifier module with an output power of 26.3 dBm, a PAE of 50%, and an adjacent channel leakage power ratio (ACLR) of −35 dBc [2] have been developed for WCDMA mobile products.