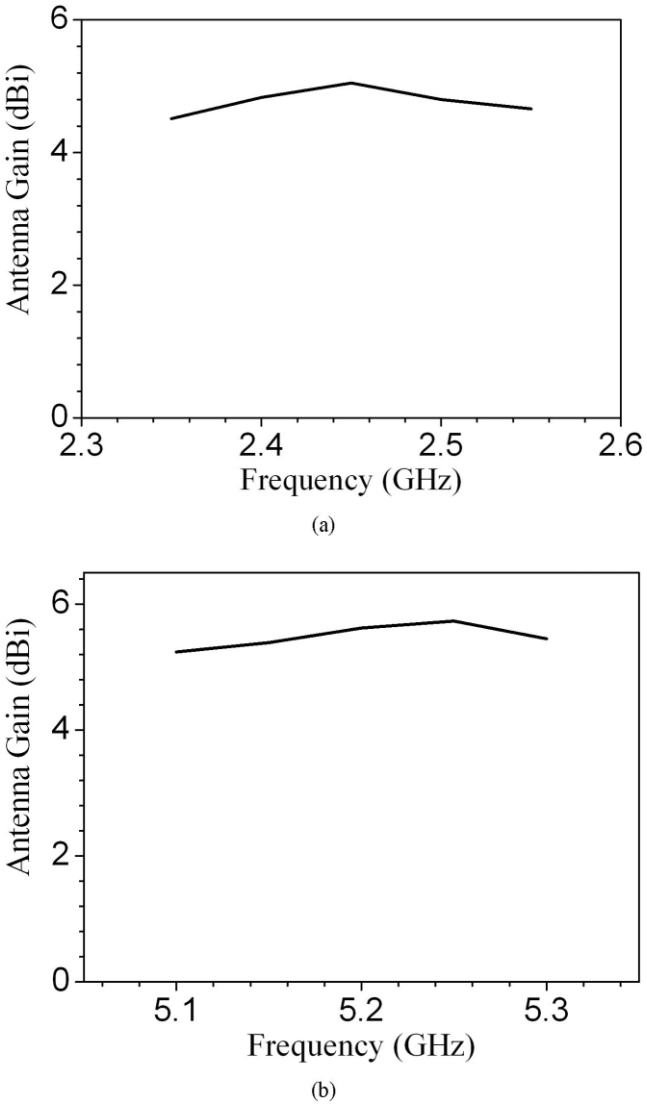

Figure 6 Measured peak gain of proposed antenna. (a) 2.4-GHz-band (2400–2484 MHz) (b) 5.2-GHz-band (5150–5350 MHz)

bands. The measured peak gains are better than 4.55 and 5.24 dBi in 2.4 and 5.2 GHz operation bands, respectively.

4. CONCLUSION

A printed T-shaped slot antenna is proposed for the dual-band WLAN operation. By using the T-shaped slot, two resonant modes are excited where one resonant mode is controlled to operate at 2.4-GHz-band and the other is controlled to operate at 5.2-GHz-band. Good agreement between the measured and simulated results verifies the design of the proposed antenna. The measured impedance bandwidths are 2.18–2.85 GHz and 4.96–5.5 GHz for VSWR ≤ 2 and are sufficient for the two bands of WLAN standard. The measured gains are better than 4.55 and 5.24 dBi at 2.4-GHz- and 5.2-GHz-Band, respectively.

ACKNOWLEDGMENTS

This work has been supported by the National Natural Science Foundation of China, under Grant No. 60571053, and the Shanghai Leading Academic Discipline Project, under Grant No. T0102.

REFERENCES

1. S.H. Yeh and K.L. Wong, Dual-band F-shaped monopole antenna for 2.4/5.2 GHz WLAN application, IEEE Antennas Propag Soc Int Symp (Digest) 4 (2002), 72–75.
2. Y.L. Kuo and K.L. Wong, Printed double-T monopole antenna for 2.4/5.2 GHz dual-band WLAN operations, IEEE Trans Antennas Propagat 51 (2003), 2187–2192.
3. C.Y. Pan, C.H. Huang, and T.S. Hong, A novel printed G-shaped monopole antenna for dual-band WLAN applications, Microwave Opt Technol Lett 45 (2003), 295–297.
4. S.Y. Lin and K.L. Wong, A dual-frequency microstrip-line-fed printed slot antenna, Microwave Opt Technol Lett 28 (2001), 373–375.
5. C.J. Wang and W.T. Tsai, A stair-shaped slot antenna for the triple-band WLAN applications, Microwave Opt Technol Lett 39 (2003), 370–372.
6. H.M. Hsiao, J.W. Wu, Y.D. Wang, J.H. Lu, and S.H. Chang, Novel dual-broadband rectangular-slot antenna for 2.4/5.2-GHz wireless communication, Microwave Opt Technol Lett 46 (2005), 197–200.

A SUBHARMONICALLY INJECTED PHASE-LOCKED LOOP FOR 5-GHz APPLICATIONS

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ABSTRACT: *This work introduces a modified subharmonic injection-locked phase-locked loop (S-ILPLL) that feeds the phase comparator with half the frequency of the voltage-controlled oscillator by employing a divider in the loop feedback path. The main objective is to address the phase noise improvement of subharmonic ILPLLs, especially for the 5-GHz band. Theoretical analysis and computer calculations demonstrate an improved performance for phase noise and power consumption. An experimental prototype was implemented to verify the validity of the proposed approach. Measurement results are in good agreement with computer calculations, thus the proposed S-ILPLL can constitute an attractive design approach for 5-GHz WLAN synthesizers.* © 2006 Wiley Periodicals, Inc. Microwave Opt Technol Lett 48: 2158–2162, 2006; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.21888

Key words: *frequency synthesizer; injection-locked oscillator; locking range; phase noise; subharmonic injection-locked phase-locked loop*

1. INTRODUCTION

Injection-locked phase-locked loops (ILPLLs) are widely used for synchronization in optical communications and for implementation of oscillators for phased-array antennas, achieving superior phase noise performance and locking range characteristics over a conventional phase-locked loop (PLL). With the advent of high-speed wireless applications at 5 GHz, there is an increasing demand for wideband, low-cost transceiver systems. A critical system, the synthesizer, must exhibit low phase noise over a wide bandwidth, fast settling time, and low spurious level. As a result, ILPLL can become a strong candidate for achieving low phase noise performance without compromising any of the other design parameters (speed, locking range, etc.) in 5-GHz broadband wireless applications.

Although there is considerable work during the last years in fundamental-frequency injection-locking PLLs (ILPLLs) [1–9],

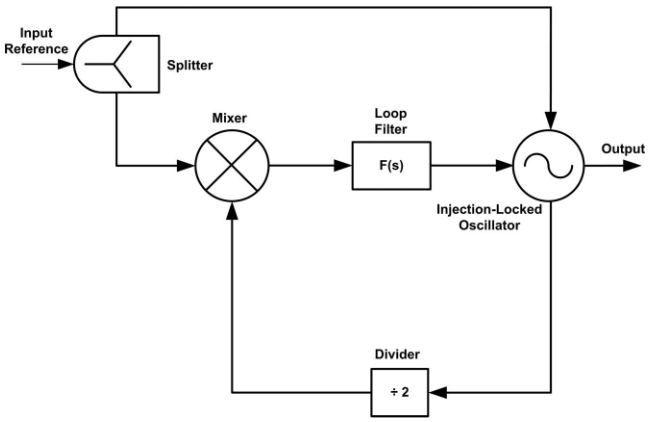

Figure 1 Subharmonic injection-locked phase-locked-loop

subharmonic-injection PLLs have only recently attracted the attention of researchers.

Studied by Zhang [10], Sturzebecher [11], and others [12, 13], this method is a combination of a PLL and an injection-locked oscillator (ILO). The voltage-controlled oscillator (VCO) of such a synthesizer is a subharmonic-injected oscillator in contrast to the free-running oscillator of the conventional PLL.

In this paper, we apply the ILPLL technique to synthesizer design for the 5-GHz band, but the literature shows that until now such an approach has not been exploited. Xue [14] introduced a 5.8-GHz injection-locked frequency synthesizer, but only experimental results are reported. Furthermore, we propose an alternative design approach where a frequency divider is placed in the loop to feed the phase comparator (balanced mixer) with a same frequency signal as the reference, as shown in Figure 1. In addition, this work examines the phase noise of subharmonic-ILPLLs, using the loop linear model, and presents the analytical expression for the locking range.

To verify the new subharmonic injection-locked phase-locked loop (S-ILPLL) concept experimentally, a prototype was implemented using commercial components. Experimental results agree with analysis, demonstrate a low phase noise system, and confirm the competitive performance of such an approach. The proposed S-ILPLL oscillator exhibits lower phase noise characteristics and is, thus, suitable for applications in broadband, mobile, and fixed wireless systems.

2. SYSTEM ARCHITECTURE

Subharmonic synchronization occurs when a VCO is injected with a reference signal (ω_{REF}) such that:

$$\omega_{REF} = \frac{\omega_o}{n} + \delta\omega, \tag{1}$$

where $n = 1, 2, 3, \ldots$ is the nonlinearity factor of the VCO, ω_o is the free-running frequency, and $\delta\omega$ is the difference between the free-running frequency and the nth harmonic of the reference frequency.

The external signal is split in two: one part is applied to the injection port of the oscillator and the second to the phase comparator realized by a harmonic mixer [12]. Another approach is proposed in Ref. 11, where a frequency multiplier is used to produce the nth harmonic of the reference signal. The nth harmonic is then injected into the phase comparator, whereas the reference signal is directly injected into the VCO. In fact, all the designs reported in literature follow the above techniques. In this paper, we follow a different approach and insert a divider in the feedback path. Current integration technology allows the implementation of low power dividers [15], making this approach very attractive for integration.

3. SYNCHRONIZATION OF THE OSCILLATOR

A common-source capacitive feedback oscillator is designed, using a low noise GaAS Hetero-Junction FET, for better phase noise performance, with a parallel resonant circuit applied at the gate. The tuning range of the oscillator is 310 MHz, from 4770 to 5080 MHz, delivering +6 dBm of output power [9].

The phase noise of the subharmonic ILO locked at the second subharmonic frequency is given by [10]:

$$L_{ILO}(\omega) = \frac{4L_{REF}(\omega)\left[\frac{\omega_O}{2Q}\frac{V_{OUT2}}{V_{OUT}}\right]^2\cos^2\varphi + \omega^2 L_{VCO}(\omega)}{\left[\frac{\omega_O}{2Q}\frac{V_{OUT2}}{V_{OUT}}\right]^2\cos^2\varphi + \omega^2}, \tag{2}$$

where φ is the stationary phase difference between the oscillator and the second harmonic of the reference signal, ω is the offset carrier frequency, ω_o is the free-running frequency, Q is the quality factor of the embedding network, V_{OUT} is the amplitude of the free-running signal, and V_{OUT2} is the amplitude of the second harmonic of the reference signal at the output of the oscillator. $L_{VCO}(\omega)$ is the single-sideband power spectral density of the phase noise of the free-running oscillator and $L_{REF}(\omega)$ is the single-sideband power spectral density of phase noise of the reference signal. φ is expressed as [1]:

$$\sin\varphi = 2Q\frac{\omega_O - 2\omega_{REF}}{\omega_O}\frac{V_{OUT}}{V_{OUT2}}, \tag{3}$$

where ω_{REF} is the reference frequency.

4. PHASE NOISE ANALYSIS AND LOCKING RANGE

4.1 Phase Noise Analysis

Figure 2 shows the linearized model for noise analysis of the S-ILPLL, where K_{VCO} and K_{PD} are the VCO and phase detector gains, respectively, ÷2 is the divider ratio, and $F(s)$ is the transfer function of the loop filter.

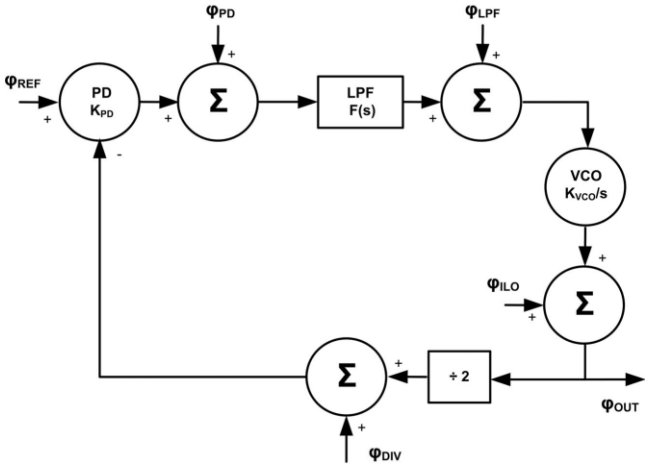

Figure 2 S-ILPLL noise model

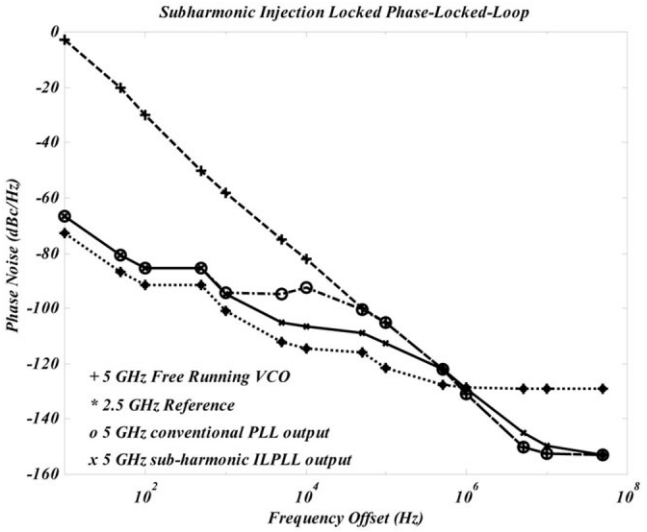

Figure 3 Calculated results for the output phase noise of the proposed S-ILPLL and a conventional PLL with the same components

Each component of the loop (ILO, phase detector, loop-filter, and divider) is taken to be the combination of a noise-free component and a source that introduces noise (φ_{ILO}, φ_{PD}, φ_{LPF}, φ_{DIV}). The total output noise φ_{OUT} is the summation of the noise produced by the ILO and the noise originating from the feedback loop (see Fig. 2). After some mathematical manipulation we get:

$$\varphi_{OUT} = (1 - H(s))\varphi_{ILO} + \frac{2}{K_{PD}}H(s)\varphi_{PD} + 2H(s)\varphi_{REF} + \\ + \frac{2}{F(s)K_{PD}}H(s)\varphi_{LPF} - 2H(s)\varphi_{DIV}, \quad (4)$$

where $G(s) = \frac{1}{2}K_{PD}\frac{K_{VCO}}{s}F(s)$ and $H(s) = \frac{G(s)}{1+G(s)}$.

Taking into account that $L_{ILO}(\omega)$, $L_{PD}(\omega)$, $L_{REF}(\omega)$, $L_{DIV}(\omega)$, $L_{LPF}(\omega)$ are the single-sideband power spectral densities of the noises φ_{ILO}, φ_{PD}, φ_{REF}, φ_{DIV}, φ_{LPF}, respectively (in units of rad^2/Hz), that each noise term is uncorrelated, and doing some rearrangements, the spectral density of the phase noise $L_{ILPLL}(\omega)$, in rad^2/Hz, of the subharmonic ILPLL is:

$$L_{ILPLL}(\omega) = \frac{4L_{REF}(\omega)\left[\frac{\omega_O}{2Q}\frac{V_{OUT2}}{V_{OUT}}\right]^2\cos^2\varphi}{\left[\frac{\omega_O}{2Q}\frac{V_{OUT2}}{V_{OUT}}\right]^2\cos^2\varphi + \omega^2}|1 - H(\omega)|^2 + \\ + \frac{\omega^2 L_{VCO}(\omega)}{\left[\frac{\omega_O}{2Q}\frac{V_{OUT2}}{V_{OUT}}\right]^2 cos^2\varphi + \omega^2}|1 - H(\omega)|^2 + 4L_{REF}(\omega)|H(\omega)|^2, \quad (5)$$

where the overall effect of $L_{PD}(\omega)$, $L_{DIV}(\omega)$, and $L_{LPF}(\omega)$ is not significant enough and has been neglected (the additive SSB phase noise is less than -120 dBc/Hz at 100 KHz offset).

Results calculated, using the method described here, are plotted in Figure 3. The reference frequency of the injected signal is set to 2.5 GHz.

The phase noise of the free-running VCO, the reference signal, and the S-ILPLL are presented by the dashed, the dotted, and the solid line, respectively. For comparison, the phase noise of a conventional PLL employing the same components is also shown (dashed–dotted line). Phase noise data for the reference signal and the free-running VCO were collected from measurements.

It should be noted that in this specific case, a peak phase noise reduction of 15 dB is observed at a frequency offset of 10 KHz compared with the conventional PLL. In general, 10–20 dB phase noise benefit can be obtained for different parameter values (loop filter characteristics). Furthermore, in a fully integrated system (where the VCO will be noisier than the one used in this work), the proposed S-ILPLL will achieve even stronger reduction of the phase noise level compared with that of a conventional PLL.

Sturzebecher [11] treats the VCO as a PLL-locked oscillator in which an injection signal is applied. For this reason, in the expression for the phase noise of an ILO (2), $L_{VCO}(\omega)$ is substituted by $L_{PLL}(\omega)$ as seen below in the second term of the numerator. The resulting phase noise now represents the phase noise of the composite S-ILPLL system:

$$L_{ILPLL}(\omega) = \frac{4L_{REF}(\omega)\left[\frac{\omega_O}{2Q}\frac{V_{OUT2}}{V_{OUT}}\right]^2\cos^2\varphi + \omega^2 L_{PLL}(\omega)}{\left[\frac{\omega_O}{2Q}\frac{V_{OUT2}}{V_{OUT}}\right]^2\cos^2\varphi + \omega^2}, \quad (6)$$

where $L_{PLL}(\omega)$ is given by:

$$L_{PLL}(\omega) = L_{VCO}(\omega)|1 - H(\omega)|^2 + 4L_{REF}(\omega)|H(\omega)|^2. \quad (7)$$

If we use the same reference signal and free-running VCO, detailed calculations of the overall phase noise from Eqs. (5) and (6) give the same results (graphically represented by the curve of Fig. 3). Consequently, the proposed analysis gives a reliable method to characterize the phase noise performance of any S-ILPLL topology.

4.2 Locking Range

Using the PLL lock equation in which the VCO is treated as an injection locked oscillator (and not as a free running source), after some mathematical manipulations, we obtain the following equation:

$$\omega_{inj} = \omega_o + \Delta\omega_{ilpll}\sin(\theta_{inj} - \varphi + \psi). \quad (8)$$

The above equation expresses the locking range of the composite S-ILPLL system. Angle φ represents the phase shift around the loop. $\Delta\omega_{ilpll}$,ψ,$\Delta\omega_{sub\text{-}ilo}$,$\Delta\omega_{pll}$ are given by the following expressions:

$$\Delta\omega_{ilpll} = \sqrt{\Delta\omega_{pll}{}^2 + \Delta\omega_{sub\text{-}ilo}{}^2 + 2\Delta\omega_{pll}\Delta\omega_{sub\text{-}ilo}\sin\varphi}, \quad (9)$$

$$\tan\psi = -\frac{\Delta\omega_{pll}\cos\varphi}{\Delta\omega_{pll}\sin\varphi + \Delta\omega_{sub\text{-}ilo}}, \quad (10)$$

$$\Delta\omega_{sub\text{-}ilo} = \frac{\omega_O}{2Q}\frac{V_{OUT2}}{V_{OUT}}, \quad (11)$$

$$\Delta\omega_{pll} = \frac{K_{VCO}K_{PD}K_{LF}}{2}, \quad (12)$$

where ω_{inj} and θ_{inj} are the frequency and the phase of the second harmonic of the reference, whereas ω_o and θ_o are the frequency and phase of the free running VCO.

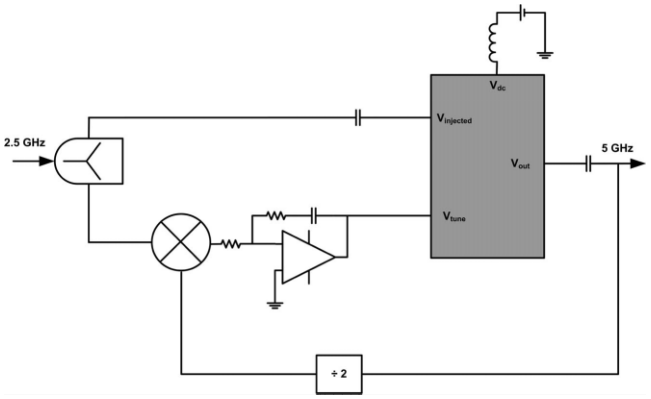

Figure 4 The implemented S-ILPLL

$\Delta\omega_{ilo}$,$\Delta\omega_{pll}$ represent the lock range of the ILO and PLL separately, whereas φ represents the phase difference in the PLL depending on the loop gain and the difference between the locked and the free running frequency.

Equation (8) is the equivalent to Adler's equation for the proposed system. Increased locking-range is obtained, larger than that of a subharmonic ILO or a conventional PLL.

5. IMPLEMENTATION AND MEASUREMENTS

To verify the above analytical results and the new S-ILPLL concept experimentally, the system shown in Figure 4 was designed and implemented. The VCO was custom designed using a low noise GaAS Hetero-Junction FET as described in Ref. 9, whereas a mixer operating in the 1.5- to 4.5-GHz range was used as phase detector. The PTFE substrate is a high frequency circuit material with an ε_r of 6.15 and a thickness of 10 mils. Impedance matching of RF inputs and outputs was realized using distributed microstripline elements. The prototype dissipates 27 mW at 3 V.

Measurements were taken for the custom-made VCO that delivers a typical output power of +7.57 dBm at 4931 MHz.

The minimum power level of the injected signal needed to establish subharmonic injection locking was found to be 31 dB below the output power of the free-running VCO. Therefore, a single band 2.5-GHz synthesizer with a typical coupled output of −25 dBm (using a built-in directional coupler) can be used to subharmonically inject the ILPLL composing a dual-band synthesizer. It is important to note that the proposed architecture makes a dual-band (2.5/5 GHz) overall system easily feasible and attractive for integration because of the low injected power necessary for subharmonic injection.

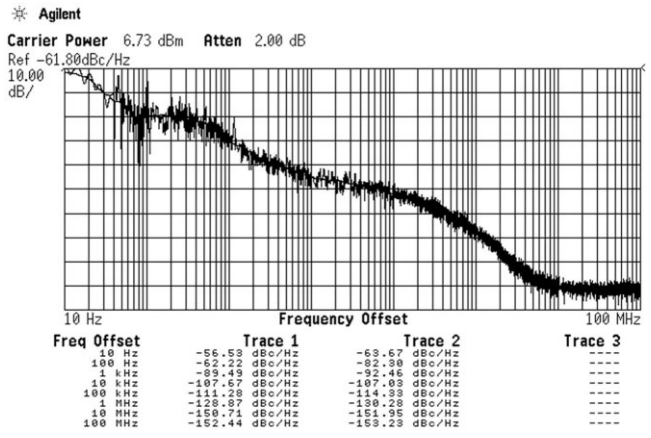

Figure 5 Phase noise measurement of the S-ILPLL

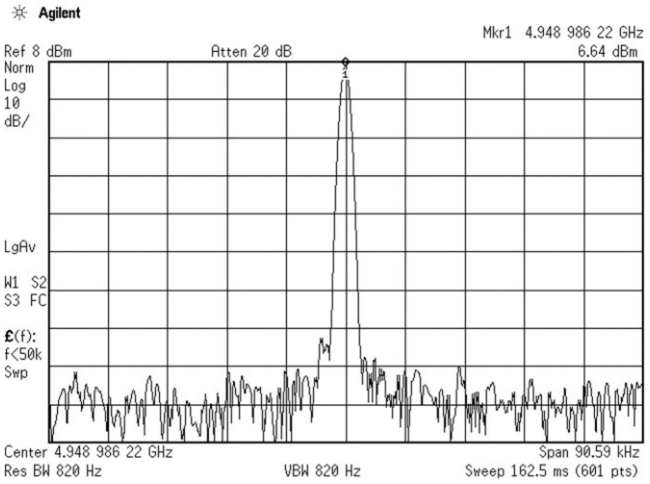

Figure 6 Output spectrum of the S-ILPLL

Figure 6 shows the measured output spectrum of the subharmonic ILPLL, whereas Figure 7 shows both measured and theoretically calculated phase noise curves for the proposed subharmonic ILPLL.

It is apparent that the measured data match the calculated data throughout the measurement band, demonstrating the high accuracy of the analysis used. In particular, the calculated results (solid line) and the measured results (dotted line) are in close agreement at high frequency offsets, whereas a peak deviation of 3.1 dB at 100-Hz frequency offset is observed.

This discrepancy is mainly due to the assumption that the contribution to the output phase noise of the phase detector noise, the loop filter noise, and the divider noise are negligible in comparison with those of the ILO and the reference signal. This assumption is not always accurate, especially for small frequency offsets (near the carrier) where the loop has little effect on the

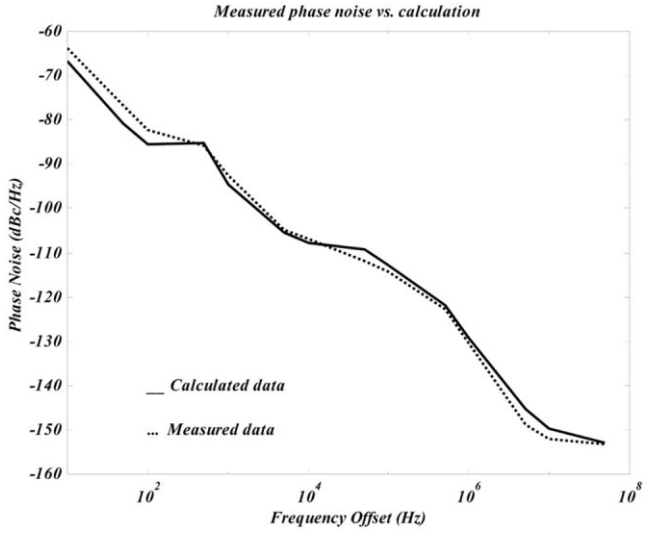

Figure 7 Measured data and calculated results for phase noise

attenuation of the phase detector noise, the loop filter noise, and the divider noise.

6. CONCLUSIONS

A modified subharmonic ILPLL for 5-GHz frequency generation was proposed, analyzed, and tested in terms of noise and locking range. It was found through analysis and measurements that the system exhibits improved phase noise performance when compared with conventional PLLs. Measurement results verified the validity of the analysis with remarkable accuracy.

It was also found that driving the main S-ILPLL with a power as low as −25 dBm at 2.5 GHz was adequate to subharmonically inject the ILPLL composing in this way a dual-band (2.5/5 GHz) synthesizer. The overall performance of the experimental design demonstrates the applicability of the proposed approach to the development of dual-band synthesizers, which constitute very important subsystems for modern multiband/multistandard transceivers.

ACKNOWLEDGMENT

The authors thank Dr. Ap. Tzimas and Mr. A. Kikis of THETA S.A. for providing the measurement platform.

REFERENCES

1. R. Adler, A study of locking phenomena in oscillators, Proc IEEE 61 (1973), 1380–1385.
2. K. Kurokawa, Injection locking of microwave solid-state oscillators, Proc IEEE 61 (1973), 1386–1410.
3. B. Razavi, A study of injection locking and pulling in oscillators, IEEE J Solid State Circ 39 (2004), 1415–1424.
4. S. Kudszus, T. Berceli, A. Tessmann, M. Neumann, and W. Haydl, W-Band HEMT-oscillator MMICs using subharmonic injection locking, IEEE Trans Microwave Theory Tech 48 (2000), 2526–2532.
5. E. Shumakher and G. Eisenstein, On the noise properties of injection-locked oscillators, IEEE Trans Microwave Theory Tech 52 (2004), 1523–1537.
6. K. Kamogawa, T. Tokumitsu, and M. Aikawa, Injection-locked oscillator chain: A possible solution to millimeter-wave MMIC synthesizers, IEEE Trans Microwave Theory Tech 45 (1997), 1578–1584.
7. F. Plessas and G. Kalivas, Locking techniques for RF oscillators at 5–6 GHz frequency range, IEEE Int Conf Electron Circ Syst 3 (2003), 986–989.
8. X. Wang, N. Gomez, L. Gomez-Rojas, P. Davies, and D. Wake, Indirect optically injection-locked oscillator for millimeter-wave communication system, IEEE Trans Microwave Theory Tech 48 (2000), 2596–2603.
9. F. Plessas and G. Kalivas, A 5-GHz injection-locked phase-locked loop, Microwave Opt Technol Lett 46 (2005), 80–84.
10. X. Zhang, X. Zhou, X. Zhang, and A. Daryoush, A theoretical and experimental study of the noise behavior of subharmonically injection locked local oscillators, IEEE Trans Microwave Theory Tech 40 (1992), 895–902.
11. D. Sturzebecher, X. Zhou, X. Zhang, and A. Daryoush, Optically controlled oscillators for millimeter-wave phased-array antennas, IEEE Trans Microwave Theory Tech 41 (1993), 998–1004.
12. S. Kudszus, M. Neumann, T. Berceli, and W. Haydl, Fully integrated 94-GHz subharmonic injection-locked PLL circuit, IEEE Microwave Guid Wave Lett 101 (2000), 70–72.
13. Y.-R. Yang and T.-H. Chu, Locking performance analysis of MESFET subharmonically injection-locked oscillator, IEEE Microwave Theory Tech 47 (1999), 1014–1020.
14. Q. Xue, A wideband subharmonically injection-locked frequency synthesizer for LMDS, Microwave Opt Technol Lett 30 (2001), 310–312.
15. S. Pellerano, S. Levantino, C. Samori, and A.L. Lacaita, A 13.5-mW 5-GHz frequency synthesizer with dynamic-logic frequency divider, IEEE J Solid State Circ 39 (2004), 378–383.

A SMALL BANDSTOP MICROSTRIP FILTER FOR UWB APPLICATIONS

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Received 4 April 2006

ABSTRACT: *A small bandstop microstrip filter for ultra-wideband application is proposed. The proposed filter combines the traditional short-circuited stub highpass filter and the open-circuited stub bandstop filter on the mitered 50-Ω microstrip line. The distributed highpass filter scheme is applied to achieve highpass filtering characteristics over ultra-wideband frequency band (3.1–10.6 GHz) and the open-circuited stubs are used to obtain the band rejection function at Wireless Local Area Network frequency band. The measured results show that the proposed filter has a wide passband characteristic of 132.12% (2.16–10.57 GHz), with the return loss of less than −10 dB and 3-dB stop band of 14.37% (5.17–5.97 GHz). The measured group delay is less than 0.65 ns within the passband except the rejection band.* © 2006 Wiley Periodicals, Inc. Microwave Opt Technol Lett 48: 2162–2165, 2006; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.21887

Key words: *bandstop filer; microstrip filter; UWB filter; wide-passband*

1. INTRODUCTION

After the Federal Communications Commission assigning the 3.1–10.6 GHz frequency band for public communications without license for ultra-wideband (UWB) applications, many researchers have extensively investigated the modern indoor wireless communication system with high data transmission rate such as sensors, radar, and tracking applications. For the reliable use of these communication services, the design of UWB devices, such as antennas, filters, and low noise amplifiers, is very important. Various types of UWB antennas operating from 3.1 to 10.6 GHz have been studied [1–3]. Because of the collocation of the UWB frequency band with frequency band reserved for WLAN (Wireless Local Area Network) frequency band over 3.1–10.6 GHz, there is a need for the wideband device to provide filtering over the WLAN frequency band so as to avoid the possible interference between the two systems.

The basic filter theories for highpass and bandstop filters are extensively investigated in [4]. However, a few filters for UWB applications have been implemented so far.

In this letter, a small bandstop microstrip filter using two short-circuited stubs and two open-circuited stubs is suggested. To obtain the highpass filtering characteristics over UWB frequency band, the distributed highpass filter with Chebyshev function is used. The characteristic impedance of each short-circuited line is initially calculated as described in [5] and modified by using 3D full-wave EM simulator [6]. The bandstop function is achieved by using two open-circuited stubs. The bandstop frequency band can be controlled by changing the length of stubs.

The proposed filter has the merits of small size and easy fabrication as well as wideband performance. Details of the proposed filter design and experimental results are presented and discussed.