Ultra wideband, low-power, 3–5.6 GHz, CMOS voltage-controlled oscillator

Athanasios Tsitouras [a], Fotis Plessas [b],*

[a] Department of Electrical and Computer Engineering, University of Patras, Patra, Greece
[b] Department of Computer & Communication Engineering, University of Thessaly, Greece

ARTICLE INFO

ABSTRACT

In this paper, a low-power inductorless ultra wideband (UWB) CMOS voltage-controlled oscillator is designed in TSMC 0.18 μm CMOS technology as a part of a ultra wideband FM (UWBFM) transmitter. The VCO includes a current-controlled oscillator (CCO) which generates output frequencies between 1.5 and 2.8 GHz and a voltage-to-current (V-to-I) converter. A low-power frequency doubler based on a Gilbert cell, which operates in weak inversion, doubles the VCO tuning range achieving oscillation frequencies between 3 and 5.6 GHz. Thus, the well-known proportionality between the oscillation frequency and the bias tuning current in CCOs is avoided for the entire achieved tuning range, resulting in a lower power design. The employed architecture provides high suppression, over 45 dB, of the 1st and 3rd harmonics, while enabling high-frequency operation and conversion gain due to the unbalanced structure and the single-ended output. The current consumption is 5 mA at a supply voltage of 1.8 V. The VCO exhibits a phase noise of −80.56 dBc/Hz at 1 MHz frequency offset from the carrier and a very high ratio of tuning range (60.4%) over power consumption equal to 8.26 dB which is essential for a UWBFM transmitter.

© 2009 Elsevier Ltd. All rights reserved.

1. Introduction

The great potential of a ultra wideband (UWB) radio lies in the fact that it is able of co-existing with the available licensed spectrum users and can still pave the way for various wireless applications with short range, high data rate [1].

However, the need for wide bandwidth complicates the circuit implementation of major RF blocks such as the transmit/receive switch, the power amplifier (PA), the low-noise amplifier (LNA), the wide tuning range VCO's and mixers in a UWB radio. CMOS technology is the preferable solution compared with other expensive technologies (SiGe, GaAs) towards a single-chip, low-cost transceiver realization. However, some inherent limitations of CMOS (low gain, low breakdown voltage, poor passive components, lack of accurate models, etc.) makes CMOS RFIC's design at such high frequencies and such a wide bandwidth a challenging task.

In [2] a novel ultra wideband FM (UWBFM) communication system was presented, promising lower complexity and power consumption when compared to the well-known UWB impulse radio system. The transmitter consists of a wideband VCO which is FM modulated (high modulating index β_{FM}) by the output signal $m(t)$ of a subcarrier VCO. The latter is FM modulated, with low modulating index β_{FM}, by a low data rate signal as it is shown in

Fig. 1b. This constant-envelope double frequency modulation technique enables the spread of the transmitted signal and multi-user operation. Phase noise performance is not so critical for a UWBFM system due to the noncoherent detection scheme of the receiver, thus it can be relaxed for lower power consumption; a maximum value of −70 dBc/Hz at 1 MHz offset was deemed satisfactory [2]. Aiming at the implementation of ultra wideband VCO circuits, the prime objective of this work is to develop an inductorless VCO scheme of very low power consumption, high gain, wide range and simple structure that could form the main block of a UWBFM transmitter. Current-controlled oscillators (CCOs) are widely used in such architectures where variable bias currents are needed to modulate the frequency. Consequently, the maximum power consumption is determined by the maximum desired frequency.

In this paper, we propose an ultra wideband, low-power, 3–5.6 GHz CMOS VCO, as shown in Fig. 1a. This VCO is designed and implemented in TSMC 0.18 μm CMOS technology. It includes a relaxation-type current-controlled oscillator which generates output frequencies between 1.5 and 2.8 GHz and a voltage-to-current (V-to-I) converter. A low-power frequency doubler based on a Gilbert cell operating in weak inversion, doubles the VCO tuning range, thus achieving oscillation frequencies between 3 and 5.6 GHz. As a result, the entire 3.1–5 GHz band is covered. The proportionality between the oscillation frequency and the tuning bias current which holds in CCOs is avoided in this case for the entire frequency range of interest, resulting in low power consumption since the CCO tuning range is doubled whereas the

* Corresponding author. +Tel.: 30 6937 072632; fax: 30 2610 911576.
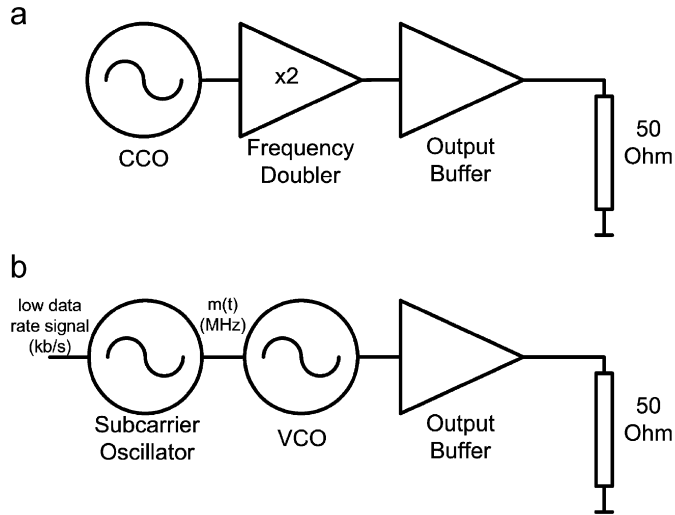E-mail address: plessas@ee.upatras.gr (F. Plessas).

a

b

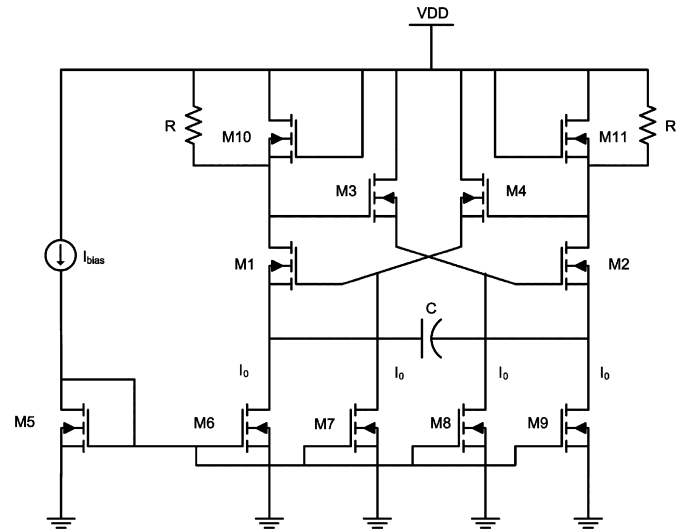**Fig. 1.** (a) The proposed designed system and (b) the complete UWBFM transmitter.

Fig. 2. Basic source-coupled multivibrator/CCO.

maximum CCO tail current is not increased by a factor of two but remains the same instead. The only disadvantage is the power consumption of the frequency doubler, which, in our case, is very low. Furthermore, the unbalanced structure of the doubler enables high-frequency operation and conversion gain. A single-ended output is used to combine high-frequency performance with adequate conversion gain. We present an analysis demonstrating that in weak inversion as this imbalance increases the conversion gain of the frequency doubler increases as well. Finally, a wideband output open-drain buffer capable of driving $50\,\Omega$ is employed. Such a VCO is suitable for UWBFM applications [2], since it is optimized for very high tuning range over low power consumption ratio and fulfills the phase noise and the output voltage variation requirement.

This paper is organized as follows. In Section 2 we discuss in great extent the selection of the specified VCO topology, the low-power frequency doubler and the output buffer. Simulation results are also given. In Section 3 we describe the overall implementation together with post layout simulation results followed by a comparison with previously published work. Finally, we provide our conclusions in Section 4.

2. Circuit design

2.1. Source-coupled multivibrator as a relaxation CCO/VCO

Source-coupled multivibrators and ring oscillators are both suitable architectures for achieving wide tuning range, however the former exhibit more stable performance over temperature and process variations. Consequently, source-coupled multivibrators allow robust circuit design.

The oscillation frequency of the classical source-coupled multivibrator (Fig. 2) is given by

$$f = \frac{I_{CAP}}{2\Delta V_{C,pk-pk}C} = \frac{I_{CAP}}{4V_{GS,ON}C}, \quad I_{CAP} = I_0 \tag{1}$$

The diode-connected transistors in Fig. 2 serve as CCO/VCO loads and as output voltage limiters. As it can be seen from (1), the oscillator in Fig. 2 can be transformed to a CCO only when the output voltage is kept constant and the tail currents vary. However, diode-connected transistors, in submicron technologies, cannot serve as good voltage limiters due to the fact that square

law is not valid anymore. In Eq. (1) it is assumed that the current through the capacitor is constant during the full oscillation period. This assumption leads to errors in the frequency estimation of a relaxation current control oscillator as it is discussed in [3] and proved in [4,5]. Eq. (1) reveals that the source-coupled multi-vibrator can be used as a CCO/VCO with wide tuning range in case that the current consumption is adequate. In [6] this oscillator topology is designed at 5 GHz and the tail current is equal to 3 mA for each current source of the CCO core. The need for lower power design can be fulfilled if the proportionality between the tail current and the oscillation frequency is violated. This can be achieved when a low-power frequency doubler is used.

The proposed relaxation-type VCO is depicted in Fig. 3. The well-known replica biasing technique [7,8] is used to keep the output voltage constant when the VCO core bias current and thus the oscillation frequency varies. A different method for keeping the output voltage of the CCO/VCO constant is to use additional compensation current sources [9–12]. Although other configura-tions of the source-coupled multivibrator were used in the past to increase the maximum oscillation frequency while maintaining the same current consumption by using an additional MOSFET switching pair [7,10–13], in our case only one switching pair is used due to the limited available headroom.

The load of this source-coupled multivibrator is formed by MP1 and MP2 which are biased in the linear region. Each one of these PMOS devices forms a bias-dependent resistance. By changing their gate bias voltage this resistance varies. The R_{SD} resistance of the PMOS device should be kept low for high-frequency VCO design. By increasing the gate width to reduce R_{SD} the gate-source capacitance and the gate-drain capacitance (linear region) of the PMOS is increased. This slows down the VCO speed, thus a compromise should be made. The basic condition for this circuit to work as a CCO/VCO is that its output voltage should be kept constant. This condition is satisfied by the replica biasing circuit (OpAmp, MP3, M3, M7). The devices MP3, M3 and M7 are scaled down (by a factor of two) compared to the MP1, M1 and M8 so that the power consumption is reduced. The VCO frequency is controlled by changing the tail bias current of the current sources M8 and M9 (and M7 as well). This is accomplished by the current mirror MP4 and M6. MP4 is biased in linear region and serves as a bias-dependent resistance which is controlled by $V_{control}$. The devices M4 and M5 serve as common-drain buffers and they are used to drive the frequency doubler.
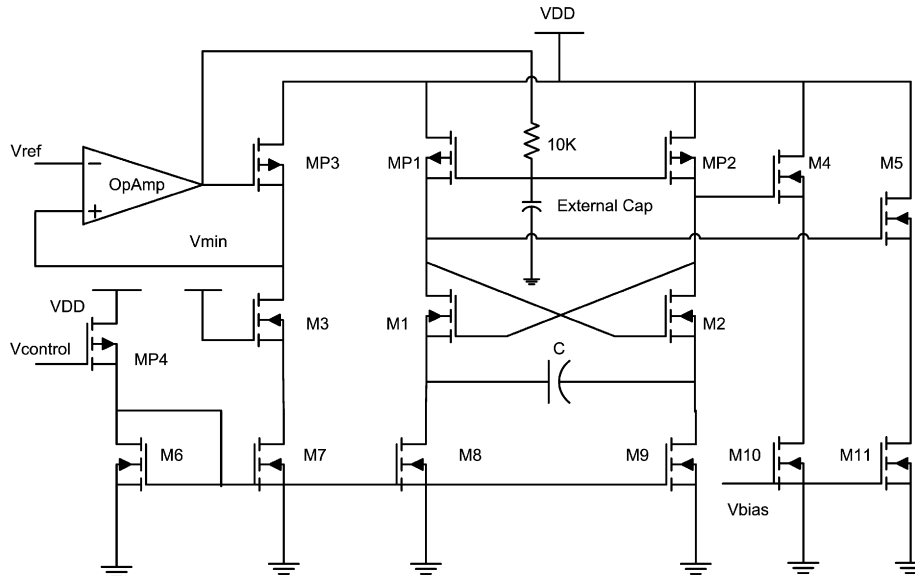
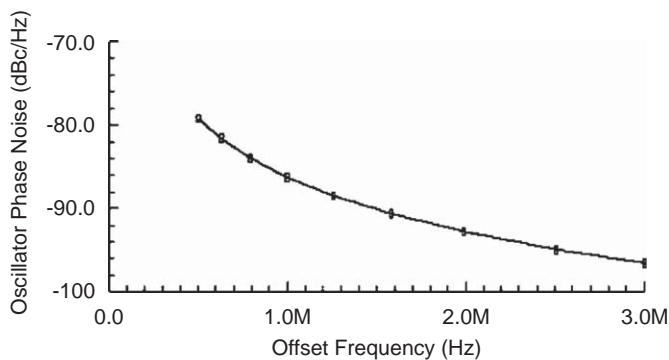Fig. 3. A relaxation-type VCO using the replica biasing technique.

Fig. 4. Phase noise of the VCO simulated at 2 GHz versus frequency offset.
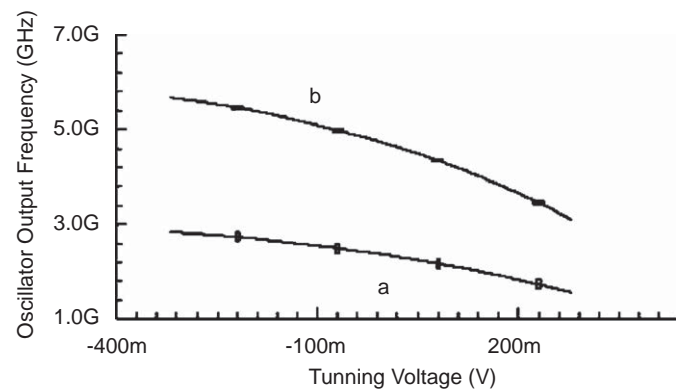

Fig. 5. PSS simulation result for the frequency versus tuning voltage characteristic for the (a) 1st and (b) 2nd harmonic component of the source-coupled multivibrator/VCO.

The width of transistors M1, M2 and MP1, MP2 of this relaxation VCO is set to 25 and 15 µm, respectively, while their length is kept minimum. The tail current sources of the VCO and the control circuit devices are the major noise contributors in this design. These transistors sizes are increased to limit their thermal and flicker noise. This results in improved phase noise performance. The VCO's maximum current consumption is 4 mA including both the output voltage control mechanism and the frequency control circuitry. The bias current provided by M8 and M9 are 1.05 and 0.61 mA at the maximum and minimum oscillation frequency, respectively. The floating capacitance C is fixed at 300 fF which is much higher than the intrinsic capacitances of the VCO core MOSFETS.

Transient simulation showed that at the maximum and minimum achievable oscillation frequency (2.8 and 1.34 GHz) a small output voltage modulation of about ± 1.2 dB exists as the frequency changes. This can be explained by the fact that at F_{MAX} (2.84 GHz) the M1, M2 switching behavior worsens slightly. The current of the VCO core (left or right branch) at 2.8 GHz switches between 1.9 and 0.2 mA and at 1.46 GHz switches between 1.16 mA and 43 µA. The switching behavior is fairly good over the entire tuning range of 1.34 GHz which ensures that current is efficiently used to tune this VCO.

In Fig. 4 the VCO phase noise at 2 GHz ($V_{control}$ equals 140 mV) is simulated versus the frequency offset. At an offset frequency of

1 MHz it is equal to -86.6 dBc/Hz. The above phase noise result is taken after the addition of the external RC filter (Fig. 3) at the gates of MP1 and MP2. Its purpose is to filter out most of the output noise (thermal and flicker) of the operational amplifier which is up-converted at the oscillation frequency band. In Fig. 5 the PSS simulation result for the oscillation frequency versus the tuning voltage is shown for the (a) 1st and (b) 2nd harmonic component of the source-coupled multi-vibrator/VCO. For a control voltage of -78 mV the VCO oscillates at 2.5 GHz, for 300 mV it oscillates at 1.5 GHz and at -320 mV the oscillation frequency is 2.8 GHz. The VCO sensitivity is equal to 2 GHz/V.

2.2. Frequency doubler selected topology

A MOS transistor operates in weak inversion when the gate-source voltage is below the threshold voltage V_T, thus the effective gate-source voltage has a negative value. In this region, the total drain current is given by Eq. (2) and the transconductance by Eq. (3) [14]. The latter shows that MOSFET in this regime behaves similarly to a bipolar transistor, thus it achieves higher transconductance. This enables low-voltage and low-current MOSFET

operation which makes this regime favorable for low-power circuit design.

$$i_D = I_S \exp\left(\frac{v_{GS} - V_T}{nV_t}\right) \tag{2}$$

$$g_m = \frac{I_{D,bias}}{nV_t} \tag{3}$$

$$I_S = 2n\mu_n C_{ox} V_t^2 \frac{W}{L} \tag{4}$$

where I_S is the specific current, V_t is the thermal voltage (25 mV at room temperature), V_T is the MOSFET threshold voltage, v_{GS} is the total gate-source voltage (DC and AC), n is the weak inversion slope factor, g_m is the transconductance and $I_{D,bias}$ is the drain bias current.

The analysis of an unbalanced Gilbert cell in the case of bipolar devices is given in [15–17], where a differential output is employed and it was proved that the differential output is free of the 1st and 3rd harmonic component. In [16], this principle is applied for a bipolar four-quadrant analog quarter-square multiplier and in [17], for a frequency mixer with a frequency doubler. MOS pseudologarithmic half-wave and full-wave recti-fiers are designed in [15] based on the same principle. In [18,19] the circuit shown in Fig. 6 is studied for both differential and single-ended output cases where M1–M4 MOSFET devices are biased in the saturation regime and a measured output bandwidth of 4 GHz (from 1 to 5 GHz) is achieved. To justify that 1st and 3rd harmonic components are cancelled when M1–M4 are biased in weak inversion regime for either single-ended or differential output, we present the foregoing analysis. Moreover, the differ-ential and single-ended conversion gain is calculated. To our best knowledge, such an analysis has not been reported in the past.

For an unbalanced common-source differential pair with MOSFETS (M1, M2) operating in weak inversion, the difference between the drain currents is given by Eq. (5) when it is biased with a tail current I and an input differential voltage v_d is applied. Note that V_K is a virtual voltage which expresses the M1 and M2 widths difference in volts. Eq. (5) will be silently used in the foregoing analysis.

$$\underset{(\times K)}{i_{D2}} - \underset{(\times 1)}{i_{D1}} = I \tanh\left(\frac{v_d + V_K}{2nV_t}\right) \tag{5}$$

$$K = \exp\left(\frac{V_K}{nV_t}\right), \quad \frac{I_{S,2}}{I_{S,1}} = \frac{W_2}{W_1} = K \tag{6}$$

The currents I_L and I_R shown in Fig. 6 are given by

$$I_L = i_{D,1} + i_{D,3} \tag{7a}$$

$$I_R = i_{D,2} + i_{D,4} \tag{7b}$$

The differential output voltage is given by

$$\Delta V_{out} = R(i_{D,1} - i_{D,4}) - R(i_{D,3} - i_{D,2}) \tag{8}$$

then,

$$\Delta V_{out} \cong IR\left(\frac{V_K}{nV_t} - \frac{V_K^3}{12V_t^3 n^3} - \frac{V_K A_d^2}{8V_t^3 n^3} - \frac{V_K A_d^2}{8V_t^3 n^3}\cos 2\omega t\right) \tag{9}$$

The differential conversion gain DCG is given by

$$DCG \equiv \frac{A_{d,out|2\omega}}{A_{d|\omega}} \cong \frac{IRA_d \ln K}{8V_t^2 n^2} \tag{10}$$

DCG is proportional to the bias current, the output load the input signal amplitude and the lnK.

The drain currents of M1–M4 are given by

$$\underset{(\times 1)}{i_{D2}} = \frac{I}{1 + \exp((-v_d + V_K)/nV_t)} \tag{11a}$$

$$\underset{(\times 1)}{i_{D4}} = \frac{I}{1 + \exp((v_d + V_K)/nV_t)} \tag{11b}$$

$$\underset{(\times K)}{i_{D1}} = \frac{I}{1 + \exp((-v_d - V_K)/nV_t)} \tag{11c}$$

$$\underset{(\times K)}{i_{D3}} = \frac{I}{1 + \exp((v_d - V_K)/nV_t)} \tag{11d}$$

From (11b), (11c) and (11a), (11d), it can be seen that V_K appears to behave as a part of the small signal input voltage. Moreover, when the unbalanced differential pairs formed by M1, M4 and M2, M3 are considered, one can observe the following: in the first case, at the left input of the circuit there is a small signal input equal to $(-v_d - V_K)/2$ and at the right input there is a small input signal equal to $(v_d + V_K)/2$. This means that an equivalent differential small input signal exists equal to $\mp(v_d + V_K)/2$. In the second case same comments hold; however the differential signal is now equal to $\mp(v_d - V_K)/2$. Since the gates of M1, M2 and M3, M4 are connected together, it can be assumed that either of these two different differential input signals is applied at the two inputs of the unbalanced Gilbert cell. The analysis continues assuming that a differential signal equal to $\mp(v_d + V_K)$ is applied. Then,

$$\underset{(\times 1)}{i_{D2}} + \underset{(\times 1)}{i_{D4}} = I_{DC,(2,4)} \cdot \left(\exp\left(-\frac{v_d + V_K}{2V_t}\right) + \exp\left(\frac{v_d + V_K}{2V_t}\right)\right) \tag{12}$$

where

$$I_{DC(2,4)} = I_{S,2}\exp\left(\frac{V_{GS} - V_T}{nV_t}\right) \tag{13}$$

by setting

$$x = \frac{v_d + V_K}{2V_t}, \quad \left|\frac{v_d + V_K}{2V_t}\right| \ll 1 \tag{14}$$

and using (13), (15) and (16)

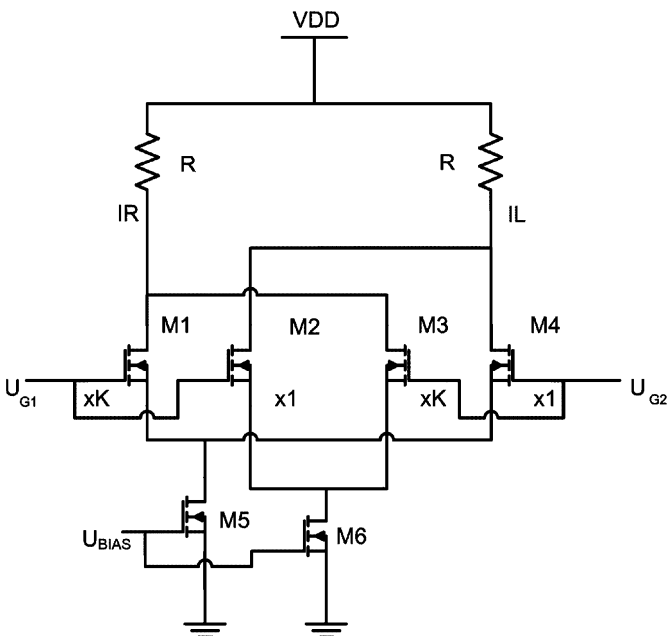$$\exp(x) \cong 1 + x + \frac{x^2}{2}, \quad |x| \ll 1 \tag{15}$$

Fig. 6. Unbalanced Gilbert cell with MOSFETS in weak inversion regime.

$$v_d(t) + V_K(t) = (A_d + V_K)\cos\omega t \qquad (16)$$

we derive (17) and (18)

$$\underset{(\times 1)}{i_{D2}} + \underset{(\times 1)}{i_{D4}} = I_{DC(2,4)}\left(2 + \left(\frac{A_d + V_K}{2V_t}\right)^2\cos^2\omega t\right) \qquad (17)$$

$$V_{out} = \left(\underset{(\times 1)}{i_{D2}} + \underset{(\times 1)}{i_{D4}}\right)R = 2I_{DC(2,4)}R + I_{DC(2,4)}R\frac{(A_d + V_K)^2}{8V_t^2 n^2}$$
$$+ I_{DC(2,4)}R\frac{(A_d + V_K)^2}{8V_t^2 n^2}\cos 2\omega t \qquad (18)$$

The single-ended conversion gain SECG is given by Eq. (19) where it can be seen that as parameter K increases, SECG increases as well.

$$SECG \equiv \frac{A_{Single-ended,\ out|2\omega}}{A_{d|\omega}}$$
$$= I_{DC(2,4)}R\frac{(A_d + V_K n \ln K)^2}{8V_t^2 n^2 A_d} \qquad (19)$$

For the frequency doubler circuit in Fig. 6 that it was used as an analog square multiplier, the MOSFETS gate widths ratio K is set to 11.25. The gate width was set to 90 and 8 μm for the large transistors (M1, M3) and the small transistors (M2, M4), respectively. The output load resistance is set to 1.5 kΩ. A polysilicon resistance was used due to its very good high-frequency performance. The MOSFETS M1, M4 and M2, M3 are both biased by the current sources M5 and M6, respectively at 0.53 mA. The gate-source voltage of M1, M2 and M3, M4 equals 578 mV, whereas the threshold voltage in this case is 600 mV. This implies that these MOSFETS are biased in the moderate inversion regime. The length of M5 and M6 is increased as much as possible (0.5 μm) in order to limit their thermal and $1/f$ flicker noise [20]. Thermal and flicker noise components of the biasing current sources of the frequency doubler will deteriorate the total phase noise of the system oscillator-frequency doubler. This effect will be added to the additional 6 dB increase of the phase noise of the system due to the frequency doubling mechanism according to the Leeson's model [21].

In Fig. 7a, the single-ended conversion gain is depicted versus the differential input signal frequency. It is equal to 0.735 V/V or −2.67 dB at the input signal frequency of 2.5 GHz. In Fig. 7b, the single-ended conversion gain versus the single input signal frequency is given. The latter equals 1.47 V/V or 3.34 dB at 2.5 GHz. The input $f_{3\,dB}$ equals to 3.26 GHz (or the output $f_{3\,dB,out}$ is 6.52 GHz) which satisfies the desired wideband behavior that our VCO demands. Fig. 8 shows the single-ended output voltage in dB versus the input signal frequency for different offset values of (a) 0 mV, (b) 20 mV and (c) 100 mV. For an offset of 20 mV the single-ended output voltage drops 0.17 dB and for an offset of
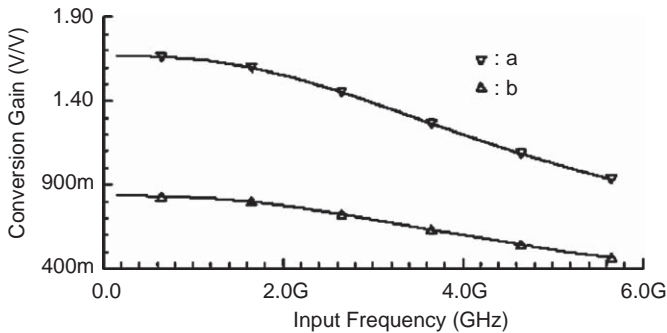

Fig. 7. (a) Single-ended conversion gain versus the single input signal frequency and (b) single-ended conversion gain versus the differential input signal frequency.
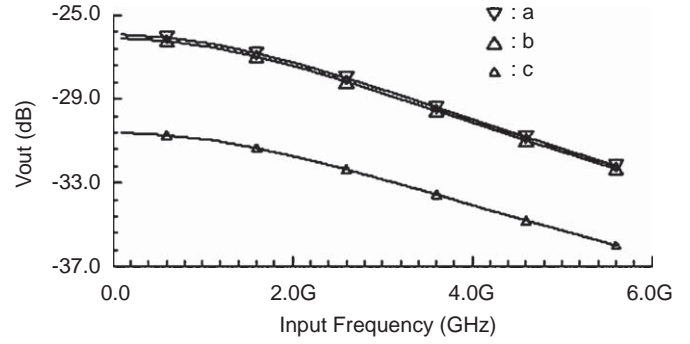

Fig. 8. Single-ended output voltage in dB versus input signal frequency for different offset values of (a) 0 mV, (b) 20 mV and (c) 100 mV.

100 mV it drops 4 dB. For the simulations results presented above, neither the input source impedance nor the loading effect at the output of the frequency doubler were taken into account.

By taking the single-ended output of this circuit wideband design can be enhanced. This happens because the single-ended output (drain of M2, M4) is taken by the output node of the circuit where the MOSFETs have small gate width (M2, M4) and simultaneously the M1, M3 gate width increase results in the increase of conversion gain (single-ended and differential) at low input frequencies. On the other hand, if the differential output is taken then due to the very large gate width of M1, M3 the $f_{3\,dB}$ of the circuit will be significantly decreased. When a single-ended output is taken then the $f_{3\,dB}$ of the circuit is only set by the gate width of M2, M4. Consequently, the motivation here is to increase the conversion gain at low frequencies without influencing or limiting the wideband behavior ($f_{3\,dB}$).

These two design parameters become independent when a single-ended output is taken. If the gate width of M1, M3 is decreased (compared to their size in the final design) whereas M2, M4 dimensions are kept constant, then a lower conversion gain (differential and single-ended) at low input frequencies is expected. In the case where the differential output is used then the $f_{3\,dB}$ of the circuit will be lower than before (in the final design) due to the presence of M1, M3 (their gate width should still be higher than that of M2, M4) at the output. Thus, the differential conversion gain becomes comparable to the single-ended conversion gain of the final design or even smaller. At lower input frequencies (lower than 2.5 GHz) a differential output may be used and the $f_{3\,dB}$ of the circuit will be mostly limited by the gate width of M1, M3 which is the largest. In this way, the differential conversion gain is doubled at low frequencies. When $f_{3\,dB}$ fulfills the desired specifications then this design option remains the best choice. The 4th harmonic component and higher harmonics are present at the frequency doubler output. Yet this does not cause a significant problem since this frequency band (6–10 GHz) can be easily filtered out by the UWB antenna.

2.3. Output buffer topology

The output buffer (Fig. 9) consists of a wideband preamplifier which drives an open-drain output cascode stage. The purpose of the preamplifier is to drive with sufficient amplitude swing the input of the output cascode stage up to the highest frequency of interest which in our application is 5 GHz or higher. Its power consumption will be determined by the required transconductance of the transistors for obtaining the desired bandwidth. It is advantageous, for wideband amplifier design, to bias the transistors at a current density near the region where the f_T is maximized. Moreover, by using small gate-width devices, the
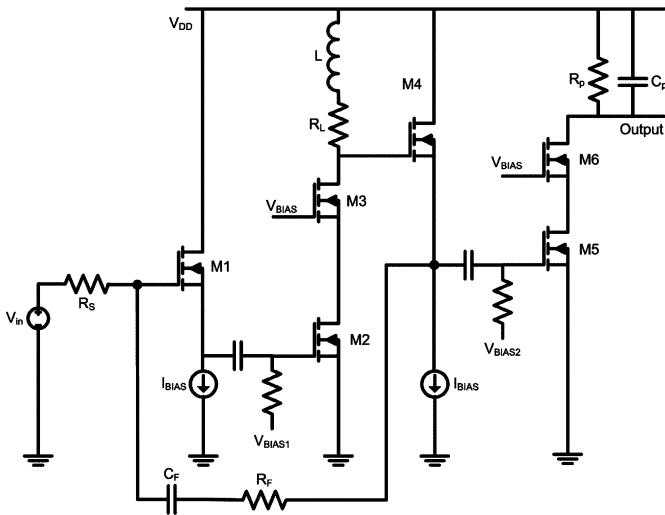
Fig. 9. Output buffer with resistive feedback and shunt-peaking inductor for extending $f_{3\,dB}$.

Fig. 10. AC simulation-output voltage of the buffer with the shunt-peaking inductor versus frequency when resistive feedback is applied at the preamplifier.

gate-source capacitance and the corresponding open time-constants are reduced.

The preamplifier is formed by a cascode stage (M2, M3) which is isolated from the input resistance R_S by an input common-drain amplifier (M1) and from the output capacitive load C_L by an output common-drain amplifier (M4). The output capacitive load C_L represents the gate-source capacitance of the output open-drain cascode stage (M5, M6). In our system the output load of the frequency doubler is in the range of kΩ and represents the input resistance R_S of the output preamplifier. The input common-drain amplifier (M1) translates the high input resistance R_S to a much smaller one (the output resistance of M1). In this way the open time-constant, which corresponds to the gate-source terminals of the input transistor M_2 of the cascode (M2, M3), is significantly decreased. The output common-drain stage (M4) of the preamplifier translates the high load resistance R_L of the preamplifier's cascode stage (M2, M3) to a much smaller resistance (the output resistance of M4). This results to the decrease of the open time-constant which corresponds to the capacitance C_L of the preamplifier. The resistance R_L should be high enough since it determines the voltage gain of the preamplifier. For these reasons this circuit can meet the specifications of a wideband amplifier design with high input resistance. The voltage gain of the cascode stage of the preamplifier is decreased by the square of the voltage gain of a common-drain amplifier, if transistors M1 and M4 are biased at the same current. However, the current gain is significantly increased due to the presence of M1 and M4. The cascode configuration is used instead of a simple common-source amplifier in order to eliminate the well-known Miller effect. Similarly, the output stage of the buffer is chosen to be a cascode amplifier as well.

For applying proper biasing conditions to devices M1–M6, two DC block capacitors and bias resistors were used. The DC block capacitors value was kept as low as possible (0.5 and 1 pF). Diode-connected MOSFETS are used as simple voltage references. The load resistance R_L of M3 was set to 1 kΩ and the output pad capacitance C_P was set to 200 fF.

In order to increase the $f_{3\,dB}$ of the output buffer, a shunt-peaking inductor was used at the first cascode stage of M2–M3. The previously mentioned voltage modulation at the VCO output in Section 2.1 can be limited by the use of the shunt-peaking inductor. Thus, an overshoot may be given to the buffer gain plot at high frequencies, if the inductor value is high enough. In
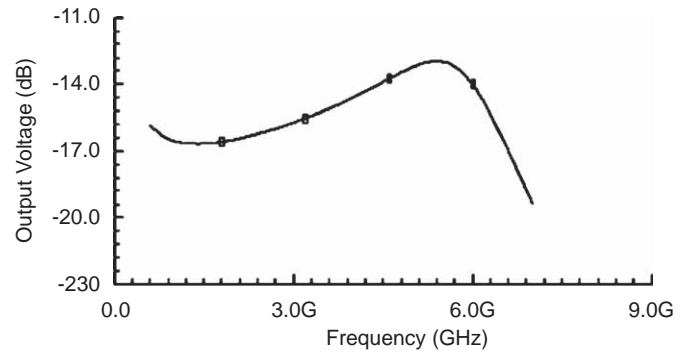
simulations, a 6.03 nH spiral inductor of the TSMC kit library was used. In the actual layout design this inductor is not included. A bondwire (1 nH/mm) is used instead so that chip area remains small. The $f_{3\,dB}$ of the output buffer with the shunt-peaking inductor is increased by 12.9%.

Furthermore, resistive feedback is applied at the preamplifier (M1–M4) via R_F (Fig. 9). The latter was set to 1.6 kΩ so that a voltage gain of approximately 1 V/V can be achieved for the preamplifier assuming that the source resistance R_S is equal to 1.5 kΩ. A DC block capacitance C_F (0.2 pF) is also used in series with R_F such that the feedback network does not draw DC current. The effect of C_F in the frequency range 3–5 GHz is small; the magnitude of Z_{CF_RF} (the series combination of R_F and C_F) equals 1.621 and 1.607 kΩ at 3 and 5 GHz, respectively.

The simulated buffer output voltage under these conditions (shunt-peaking inductor and resistive feedback) is shown in Fig. 10 for an input voltage of 200 mV pk. The fact that the voltage amplitude increases with frequency was intentionally made by proper selection of R_F, C_F and L. As the output voltage amplitude of the frequency doubler and of the VCO drops with frequency, the buffer voltage gain over the desired frequency range increases. This results in relatively constant amplitude of the buffer output voltage when the two subsystems (VCO—frequency doubler and output buffer) are connected together. The buffer voltage gain for a source resistance of 1.5 K is equal to 1.092 V/V (0.768 dB) at 5 GHz and it is equal to 0.815 V/V (−1.776 dB) at 3 GHz. The voltage amplitude at buffer's output equals −15.75 dB (or 163 mV) at 3 GHz and −13.21 dB (or 218.5 mV) at 5 GHz when a 200 mV pk input voltage is applied.

Finally, it should be noted that the last stage of the output buffer (M5, M6) is considered here as an open drain cascode stage. Thus the 50 Ω load represents the measurement instrument characteristic impedance. If an RF chock inductor is available (in case the chip is mounted on a PCB), then the instrument probe or the antenna could be directly connected at the buffer output through a DC block capacitor.

3. Implementation and system simulation results

The chip layout design is depicted in Fig. 11. The total chip area is 0.7×1.1 mm^2. The pads that were used for biasing purposes occupy $80 \times 80 \,\mu$m^2 whereas the output pad, where the output buffer is connected, occupies only $50 \times 50 \,\mu$m^2 so that its parasitic capacitance is small enough. It should be noted that the output buffer supply voltage is connected to a different pad (VDD$_{PA}$) and is isolated by the rest of the supply pads (VDD) of the circuit in order to make easier the measurements procedure. Two more pads (CAP$_{EXT}$, IND$_{EXT}$) are added for being able to connect the
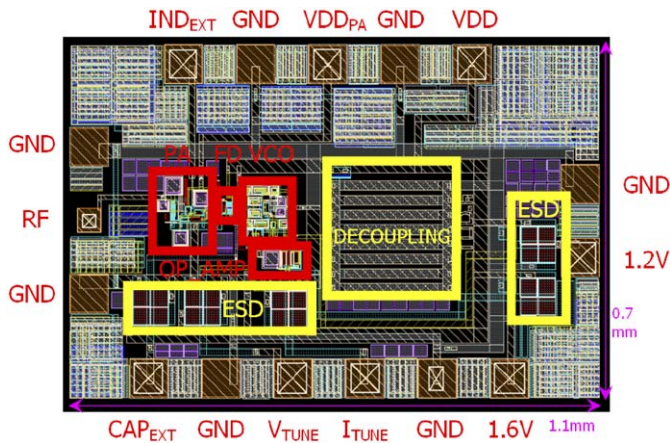
Fig. 11. Final layout design of the proposed system (VCO using the replica biasing technique, frequency doubler, output buffer and operational amplifier).

Table 1
Summary of schematic simulation results for the full system.

VCO–FD–buffer	1st harmonic	2nd harmonic	3rd harmonic
V_{OUT} (dB) at f_{2nd} = 2.943 GHz	−62	−14 (200 mV)	−62
V_{OUT} (dB) at f_{2nd} = 5.016 GHz	−63	−15.38 (170 mV)	−74.8

external capacitance to the VCO (for improving phase noise performance) and the bondwire (length: 6 mm, L: 6 nH) to the drain of the intermediate cascode stage of the output buffer. Apart from the pad which is used for the VCO tuning (V_{TUNE}), one more pad (I_{TUNE}) is connected to the gate of the tail biasing current sources of the VCO. This allows the VCO to be tuned by a current source.

Large diodes ($70 \times 70 \, \mu m^2$) are used for ESD protection of MOSFET gate nodes which are connected outside the IC. The VCO floating capacitance (MIM, 300 fF) was divided into two halves. These two half capacitors were cross-coupled for minimizing the effects of oxide gradients on capacitor matching and for providing protection against stress and thermal gradients.

For the supply decoupling, a six-metal layer capacitor ($273 \times 229 \, \mu m^2$) with 8 fingers in total was designed and connected in series to a metal resistance of $2 \, \Omega$. The total decoupling capacitance value is 8.14 pF.

The performance of the full system is summarized in Table 1. The simulated system output voltage spectrum is depicted in Fig. 12. It can be seen that the 1st and 3rd harmonic components are highly suppressed and that the voltage modulation of the output voltage at the $50 \, \Omega$ load is limited. The output voltage modulation produced only by the CCO and the frequency doubler is ± 1.5 dB within the 3–5 GHz band.

Post layout simulation results reveal that the maximum output frequency lowers about 300 MHz. The 1st and 3rd harmonics are highly suppressed at approximately the same level compared to the schematic simulations. At 2.9 GHz the V_{OUT} is 195 mV and at 5 GHz the V_{OUT} is 140 mV. The voltage modulation at the output increases slightly due to the bandwidth limitations of the output buffer and the parasitics at the output of the frequency doubler. However, the latter does not deteriorate the achieved wide tuning range of the designed VCO and frequency doubler.

A performance comparison between the VCO presented in this paper and some other published results for wideband VCOs are given in Table 2. The figure-of-merit (FOM) factor in Eq. (20) is used to compare the VCOs performance when phase noise and
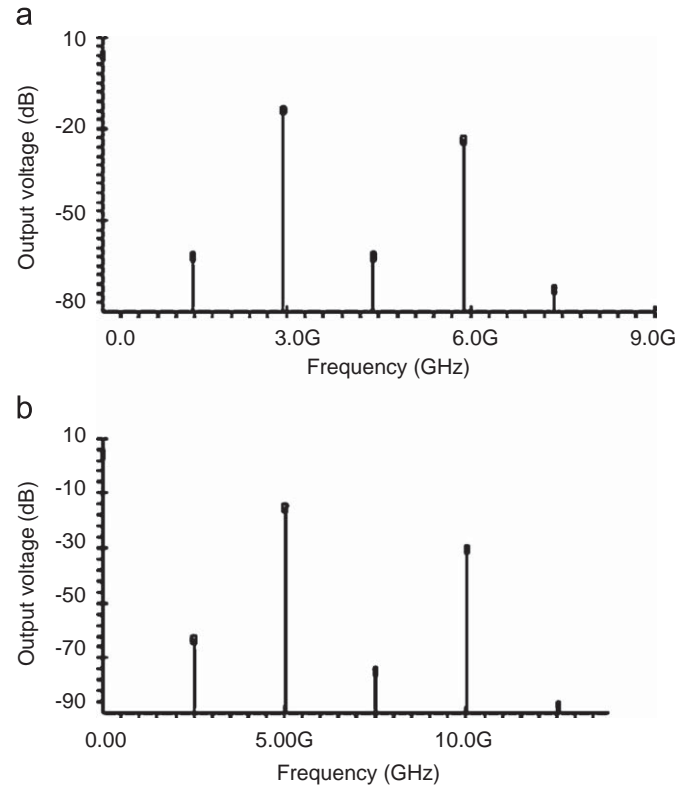
Fig. 12. Simulated system output voltage spectrum, 2nd harmonic component frequency is (a) 2.943 GHz and (b) 5.016 GHz.

power consumption are taken into account. However, a better comparison among wideband VCOs, designed for UWBFM applications, can be made when the ratio of tuning range over power consumption is calculated. The latter can be derived by Eq. (21). Although our VCO FOM is not of the highest ones, it should be stressed that it exhibits comparable to the highest ones reported, regarding the ratio of tuning range over power consumption (TR/P_{DC} equals 6.711 or 8.26 dB) set as the main design objective of this work. This provides satisfactory phase noise performance which meets the UWBFM transceiver requirement.

$$FOM = L(\Delta\omega)\left[\frac{dBc}{Hz}\right] - 20\log\left(\frac{\omega_0}{\Delta\omega}\right) + 10\log\left(\frac{P_{DC}(mw)}{1 \, mw}\right) \quad (20)$$

$$\text{Ratio of } TR \text{ over } P_{DC}, (in \text{ dB}) = 10\log\left(\frac{TR \, (in\%)}{P_{DC} \, (mw)}\right) \quad (21)$$

4. Conclusions

The design and implementation of a low power, CMOS CCO/VCO was presented, working at frequencies between 1.5 and 2.8 GHz and a low-power frequency doubler was used to double the VCO tuning range between 3 and 5.6 GHz. Concerning an UWB VCO/CCO, the concept of using a frequency doubler extends the tuning range whereas it limits the maximum current consumption. Therefore, a wideband, low-power frequency doubler design becomes an attractive solution since the total current consumption of the system (VCO/CCO and frequency doubler) is expected to be lower than in the case where the maximum tuning current of the VCO/CCO is increased in order to achieve the desired maximum frequency without the use of the doubler. The selected topology of the frequency doubler was analyzed in weak inversion

Table 2
Performance comparison of wideband voltage-controlled oscillators.

References	Technology	Inductorless	Phase Noise L (dBc/Hz) at Δf offset	Oscillation frequency Fo (MHz)	Δf offset (MHz)	Pdc (mW)	Tuning range TR (%)	FOM	TR/Pdc (dB)
[7]	0.8 μm CMOS	Yes	–	786.5	–	19.8	42	–	3.265
[11]	0.35 BiCMOS	No	−98.2	3600	0.6	42	44.4	−157.53	0.241
[12]	0.35 BiCMOS	No	−113	4300	0.6	36.5	46	−174.48	1.004
[22]	0.18 μm CMOS	Yes	−66	745	2	5.4	28	−110.09	7.147
[23]	0.25 μm CMOS	No	−98.5	1600	0.4	59	98	−152.83	2.203
[24]	0.18 μm CMOS	Yes	−75	2750	1	10.5	163	−133.57	11.909
[25]	0.18 μm CMOS	Yes	−70	3400	1	14	41.2	−129.16	4.687
[26]	0.18 μm CMOS	Yes	−90	4050	1	18.4	66.7	−149.50	5.593
[27]	0.18 μm CMOS	Yes	−90.1	3600	1	17	70.1	−148.92	6.152
This work	0.18 μm CMOS	Yes	−80.56	4300	1	9	60.4	−143.12	8.267

regime and formulas were derived to prove the related trade-offs in this region which allow low-power and high-frequency operation. Finally, a wideband output open-drain buffer was employed to drive a 50 Ω load.

The CCO maximum current consumption is 4 mA from a 1.8 V power supply including both the output voltage control mechanism and the frequency control circuitry. The frequency doubling circuit draws only 1 mA and the output buffer draws 6 mA. The proposed inductorless, low-power, wideband, CMOS VCO achieves a phase noise of −80 dBc/Hz at 1 MHz frequency offset, a wide tuning range of 60.4% and an output voltage modulation of ±1.5 dB over the desired frequency range while it consumes 9 mW. This VCO performance fulfills the requirements of UWBFM applications where the phase noise performance is not so critical and thus it can be relaxed for achieving a higher ratio of tuning range over power consumption.

References

[1] T. Barret, History of ultra wideband (UWB) radar & communications: pioneers and innovators, in: Progress in Electromagnetics Symposium, 2000, pp. 1–42

[2] J.F.M. Gerrits, M.H.L. Kouvenhoven, P.R. van der Meer, J.R. Farserotu, J.R. Long, Principles and limitations of ultra-wideband FM communications systems, EURASIP Journal on Applied Signal Processing, Special issue on UWB State-of-the-Art 3 (2005) 382–396.

[3] B. Razavi, A Study of phase noise in CMOS oscillators, IEEE Journal of Solid-State Circuits 31 (1996) 331–343.

[4] A. Buonomo, A. Sciavo, Analysis of emitter (source)-coupled multivibrators, IEEE Transactions on Circuits and Systems I 53 (2006) 1193–1202.

[5] I. Finvers, I.M. Filanovsky, Analysis of source-coupled CMOS multivibrator, IEEE Transactions on Circuits and Systems 35 (1998) 1182–1185.

[6] L.B. Oliveira, A. Allam, I.M. Filanovsky, J. Fernades, On Phase Noise in Quadrature Cross-Coupled Oscillators, in: Proceedings ISCAS, 2005, pp. 2635–2638.

[7] B. J. Song, H. Kim, Y. Choi, W. Kim, A 50% Power Reduction Scheme for CMOS Relaxation Oscillator, in: Proceedings AP-ASIC '99, 1999, pp. 154–157.

[8] B. Razavi, Design of Analog CMOS Integrated Circuits, first edition, McGraw-Hill, New York, 2000.

[9] N. Tchamov, A. Popov, P. Jarske, New Low-Power/High Speed Double-Cross-Coupled ICO/VCO, in: Proceedings MTTWA, 1997, pp. 157–158.

[10] A. Popov, N. Tchamov, P. Jarske, New High Speed Double Cross-Coupled ICO/VCO, in: Proceedings ICECS '96, 1996, pp. 243–246.

[11] P. Vaananen, M. Metsanvirta, N. Tchamov, A 3.6 GHz double cross-coupled multivibrator VCO with 1.6 GHz tuning, IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing 48 (2001) 79–802.

[12] P. Vaananen, M. Metsanvirta, N. Tchamov, A 4.3 GHz VCO with 2 GHz tuning range and low phase noise, IEEE Journal of Solid-State Circuits 36 (2001) 142–146.

[13] N. Tchamov, A. Popov, P. Jarske, VCO with Double Cross-Coupled High-Speed and Low-Power Multivibrator Architecture, in: Proceedings ISCAS '96, 1996, pp. 45–48.

[14] R. Hogervorst, Design of Low-Voltage Low-Power CMOS Operational Amplifier Cells, Ph.D. Thesis, TU Delft, 1996.

[15] K. Kimura, Some circuit design techniques for bipolar and MOS pseudologarithmic rectifiers operable on low supply voltage, IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications 39 (1992) 771–777.

[16] K. Kimura, A bipolar four-quadrant analog quarter-square multiplier consisting of unbalanced emitter-coupled pairs and expansions of its input ranges, IEEE Journal of Solid-State Circuits 29 (1994) 46–55.

[17] K. Kimura, H. Asazawa, Frequency mixer with a frequency doubler for integrated circuits, IEEE Journal of Solid-State Circuits 29 (1994) 1133–1137.

[18] M. Deen, R. Murji, A. Fakhr, N. Jafferalli, W. Ngan, Low power CMOS integrated circuits for radio frequency applications, IEE Proceedings Circuits, Devices and Systems 152 (2005) 509–522.

[19] R. Murji, M. Deen, Design issues of a low power wideband frequency doubler implementation in 0.18 μm CMOS, Analog Integrated Circuits and Signal Processing 53 (1) (2007) 53–62.

[20] A. Jerng, C. Sodini, The impact of Device Type and Sizing on Phase Noise Mechanisms, in: Proceedings CICC, 2005, pp. 547–550.

[21] D. Leeson, A simple model of feedback oscillator noise spectrum, Proceedings of the IEEE 54 (1966) 329–330.

[22] Y. Zheng, C. Saavedra, Compact CMOS VCO using a transistor for frequency control, ANTEM/URSI International Symposium on Antenna Technology and Applied Electromagnetics, Montreal, Canada, July 2006, pp. 115–118.

[23] M.A. Do, R.Y. Zhao, K.S. Teo, J.G. Ma, New wideband CMOS LC voltage-controlled oscillator, IEE Proceedings-Circuits, Devices and Systems 150 (5) (2003).

[24] A. Georgiadis, M. Detratti, A linear, low-power, wideband CMOS VCO for FM-UWB applications, Microwave and Optical Technology Letters 50 (7) (2008) 1955–1958.

[25] T. Tong, Z. Wenhua, J. Mikkelsen, T. Larsen, A 0.18 μm CMOS low power ring VCO with 1 GHz tuning range for 3–5 GHz FM-UWB applications, in: Proceedings of the IEEE 10th International Conference on Communication Systems, 2006, pp. 1–5.

[26] C.-C. Wei, H.-C. Chiu, W.-S. Feng, An ultra-wideband CMOS VCO with 3–5 GHz tuning range, in: Proceedings of the IEEE International Workshop on Radio-Frequency Integration Technology, 2005, pp. 87–90.

[27] W. Tu, J. Yeh, H. Tsai, C.Wang, A 1.8 V 2.5–5.2 GHz CMOS dual input two stage ring VCO, In: Proceedings of the IEEE Asia-Pacific Conference on Advanced System Integrated Circuits, 2004, pp. 134–37.